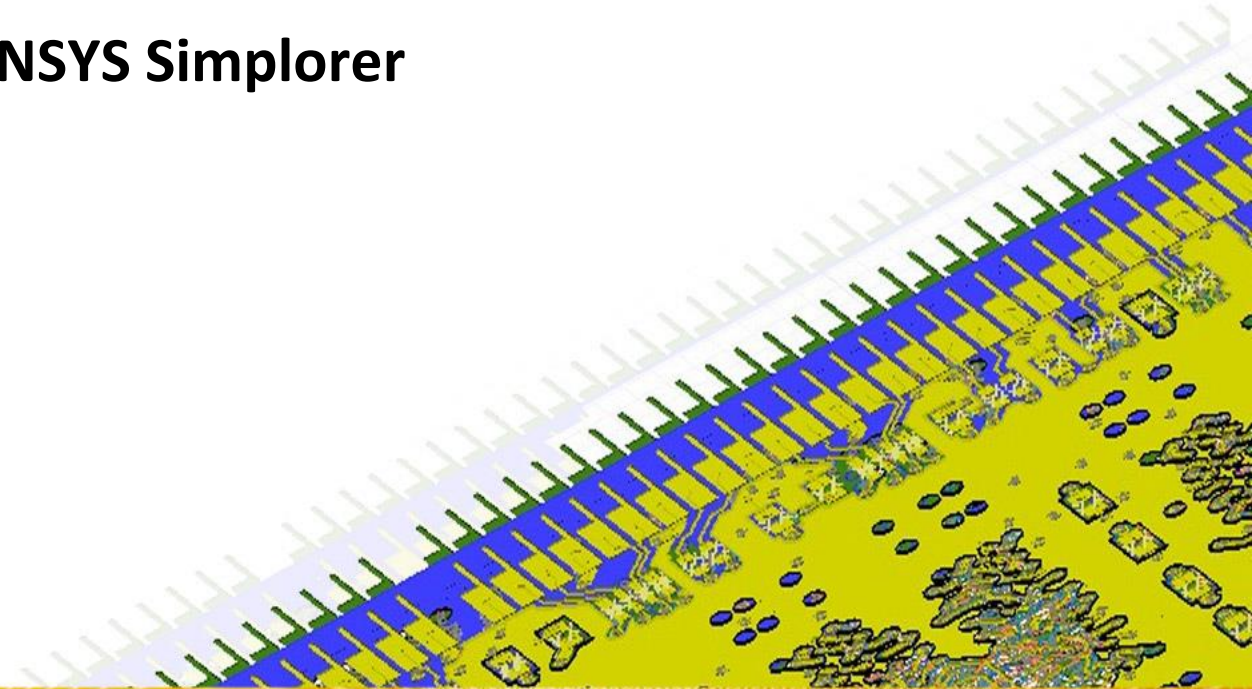




Module 03: Sub-circuits and Transfer Functions

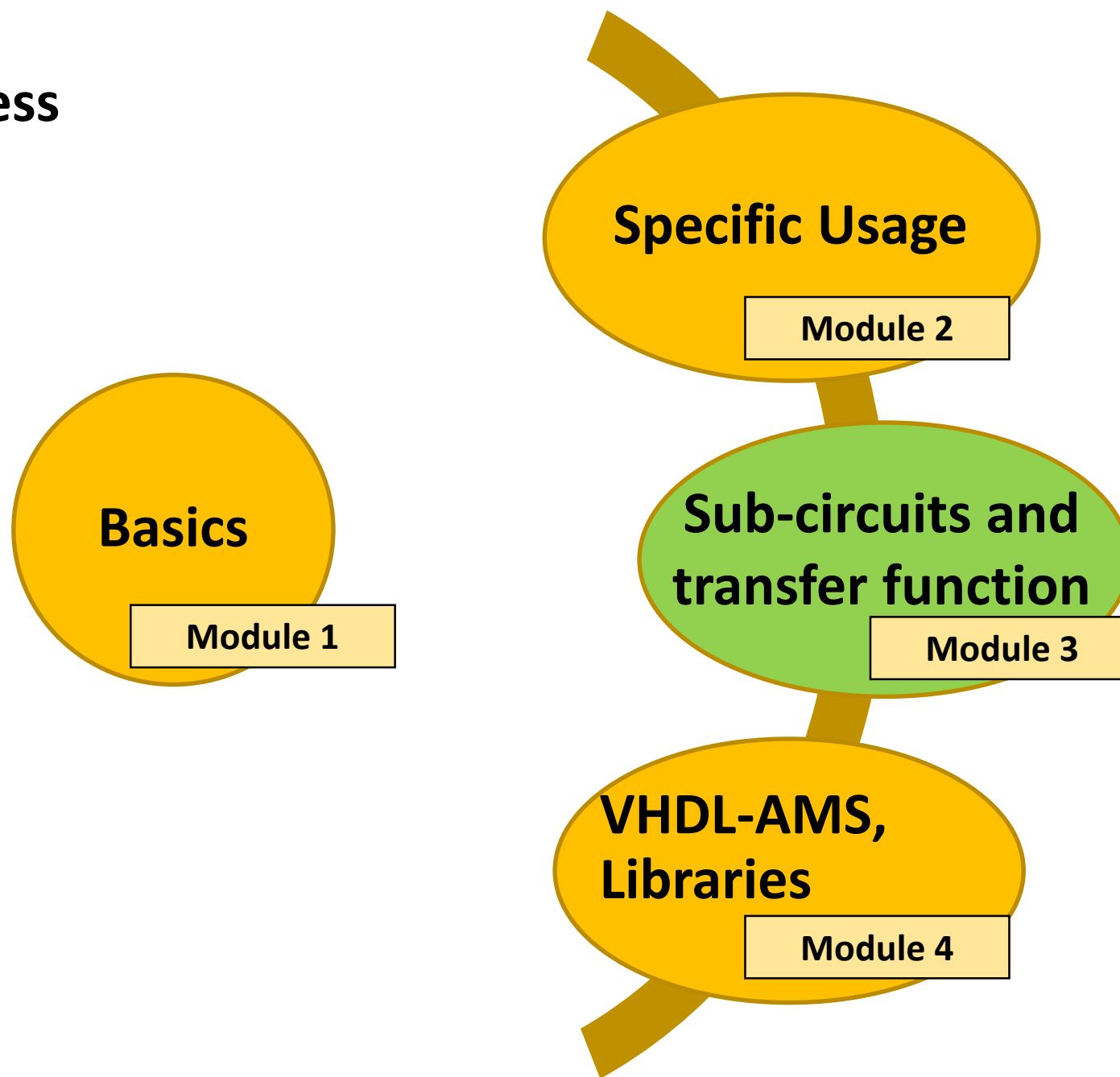
Introduction to ANSYS Simplorer





Overview

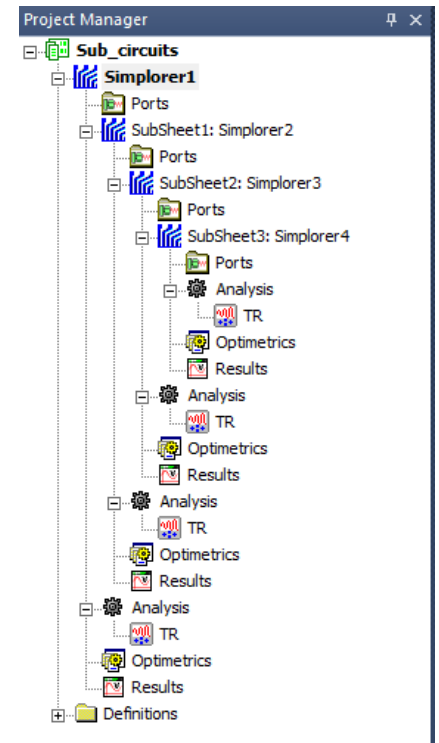
- **Sub – Circuits**
 - How to create a sub-circuit
 - Port-components
- **Transfer Functions and Blocks**
 - G(s) Block
 - Differences between yellow (SML) and blue (VHDL-AMS) blocks
 - Overview on the default blocks
- **Post-Processing II**
- **Workshop 3.1: Control Blocks**
- **Workshop 3.2: Sub-circuit**

Overall Process



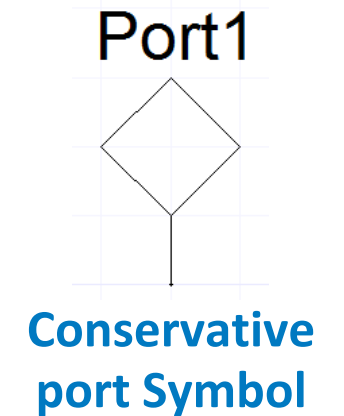
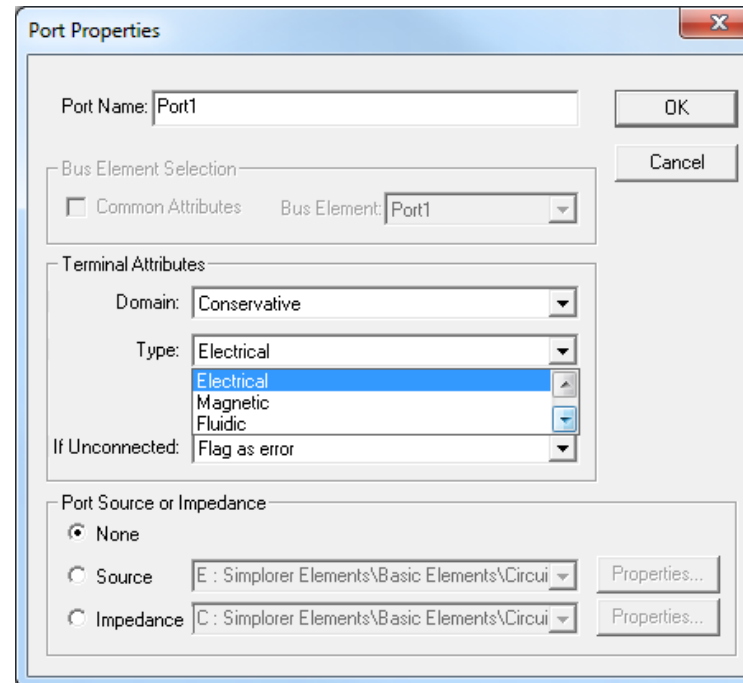
Sub-Circuits

- Simplorer hierarchy
 - Simplorer allows users to create sub-circuits (or sub-sheets) to represent complicated circuitry through different hierarchical levels of details
 - The Schematic present as default when inserting a new Simplorer Design represents the top hierarchical level
 - Nested sub-circuits are allowed
 - Simplorer offers two different ways to create sub-circuits:
 - From the menu item *Simplorer Circuit* → *SubCircuit* → *Add SubCircuit*
 - From the menu item *Schematic* → *Create SubCircuit from Selection Area*
 - If sub-levels are present, user can navigate and move between them using the “Push Down”  and “Pop Up”  icons placed in the toolbars or through the menu items *Schematic* → *Push Down* and *Schematic* → *Pop Up*
 - Dedicated components called “*Interface Ports*” play the role of interfaces, allowing signals and quantities to be transferred between different sub-levels



Interface Ports

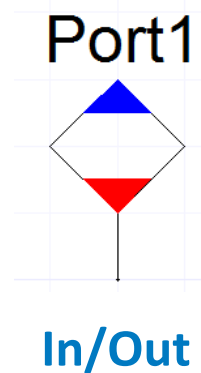
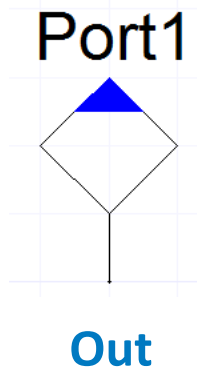
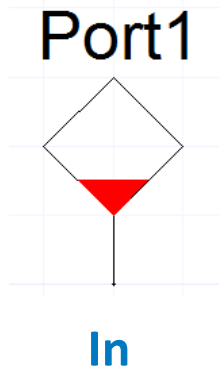
- Ports can have different Terminal Attributes, depending on Domain and Types
- Domains are **Conservative**, **Quantity**, **Signal**, **Parametric**
- Types for **Conservative Domain** are (the Port in that case represents a conservative node):
 - Electrical
 - Magnetic
 - Fluidic
 - Translational
 - Translational_velocity
 - Rotational
 - Rotational_velocity
 - Radiant
 - Thermal
 - Compressible Fluidic
- No further properties are needed



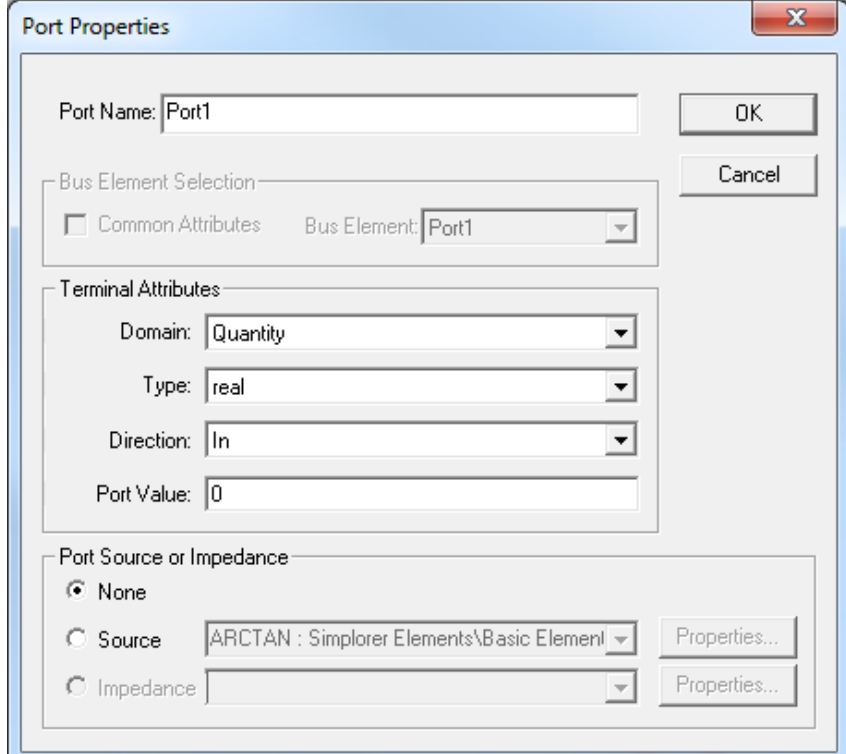
Note: Parametric is legacy coming from older Simplorer versions

Interface Ports

- Types for **Quantity Domain** are (the port behaves as a connector for pure mathematical quantities – analog components):
 - real
- In this case the port **Direction** needs to be defined:
 - In
 - Out
 - In/Out
- The Port symbol changes depending on the chosen direction



- Also the Port **Value** has to be set



Port Properties

Port Name: Port1

Bus Element Selection

☐ Common Attributes Bus Element: Port1

Terminal Attributes

Domain: Quantity

Type: real

Direction: In

Port Value: 0

Port Source or Impedance

☒ None

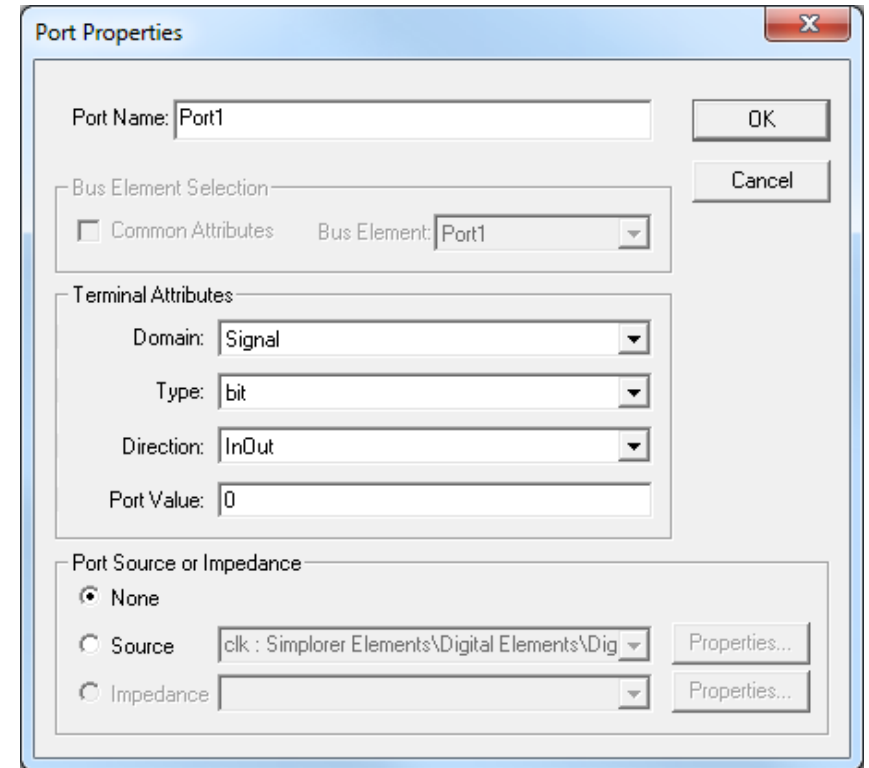
☐ Source ARCTAN : Simplorer Elements\Basic Element

☐ Impedance

OK Cancel

Interface Ports

- Types for **Signal Domain** are (the port behaves as a connector for digital components):
 - bit
 - std_logic
- In this case the port **Direction** needs to be defined:
 - In
 - Out
 - In/Out
- The Port symbol changes depending on the chosen direction as shown previously
- Also the Port **Value** has to be set



The screenshot shows the 'Port Properties' dialog box. It has a title bar with a close button. The dialog is divided into several sections:

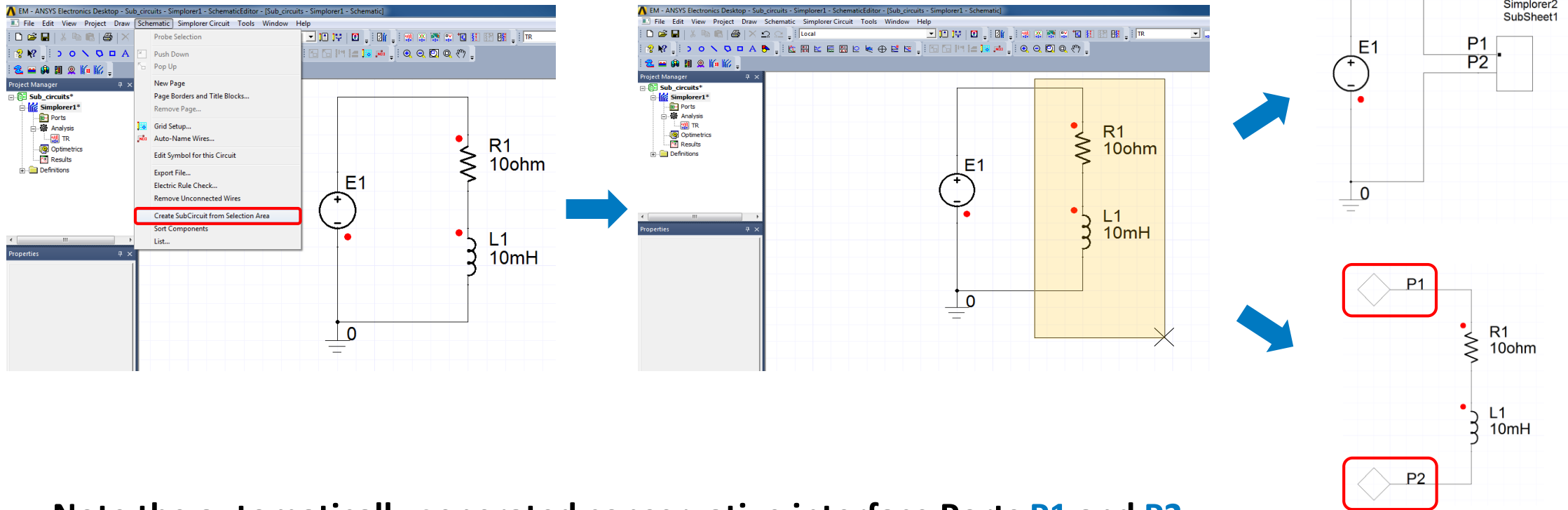
- Port Name:** A text field containing 'Port1'.
- Bus Element Selection:** A section with a checkbox for 'Common Attributes' (unchecked) and a dropdown menu for 'Bus Element' set to 'Port1'.
- Terminal Attributes:** A section with four dropdown menus: 'Domain' set to 'Signal', 'Type' set to 'bit', 'Direction' set to 'InOut', and 'Port Value' set to '0'.
- Port Source or Impedance:** A section with three radio buttons: 'None' (selected), 'Source', and 'Impedance'. The 'Source' and 'Impedance' options have dropdown menus and 'Properties...' buttons next to them.

Buttons for 'OK' and 'Cancel' are located on the right side of the dialog.

Sub-Circuits

- Create SubCircuit from Selection Area

- Using the “**Create SubCircuit from Selection Area**” command is useful to automatically create a subcircuit with the interface ports already set the right way.
- To access that command select the menu item *Schematic → Create SubCircuit from Selection Area*

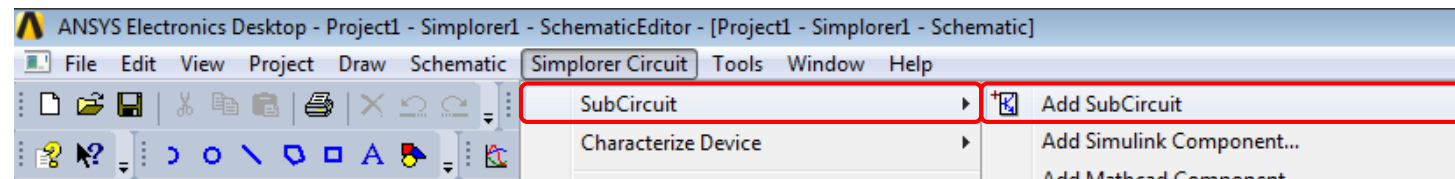


- Note the automatically generated conservative interface Ports **P1** and **P2**

Sub-Circuits

- Add SubCircuit

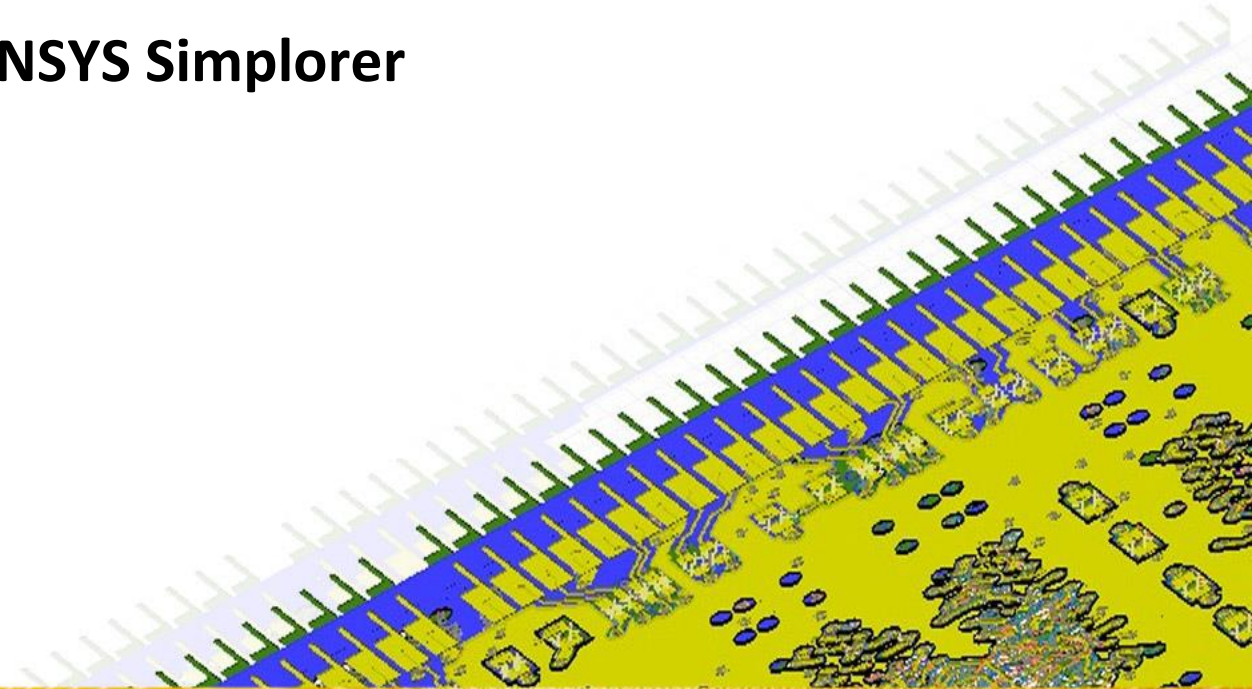
- Using the “**Add SubCircuit**” command is a good approach to set an initial complex Design structure, preparing all the needed Sub-circuits and filling them afterwards
- In that case the user has to manually add all the needed interface Ports (Conservative, Quantity, etc. with their related **types**, **directions**, etc.) to assure the right transfer of information between different sub-levels
- The command can be accessed selecting the menu item **Simplorer Circuit** → **SubCircuit** → **Add SubCircuit**





Transfer Functions and Blocks

Introduction to ANSYS Simplorer



Transfer Function

- Behavioral description in general in time-domain by ODE

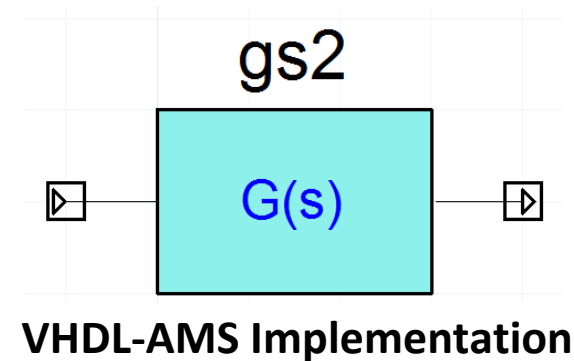
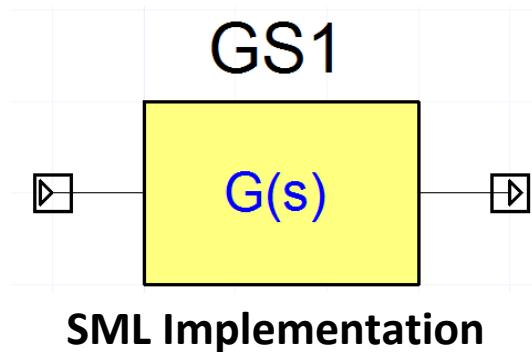
- Coefficients non-constant, nonlinear:

$$a_0y + a_1\dot{y} + a_2\ddot{y} + \dots + a_my^{(m)} = b_0x + b_1\dot{x} + b_2\ddot{x} + \dots + b_nx^{(n)}$$

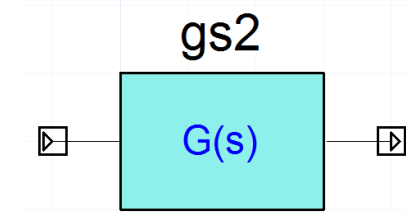
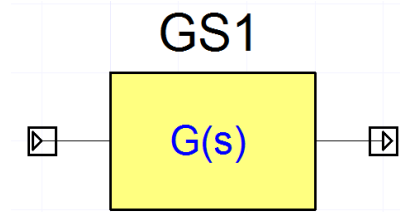
- Representation in Laplace domain (complex variable s):

$$Y(s) = \frac{b_ns^n + \dots + b_2s^2 + b_1s + b_0}{a_ms^m + \dots + a_2s^2 + a_1s + a_0}X(s)$$

- Representation in Simplorer:



Transfer Function



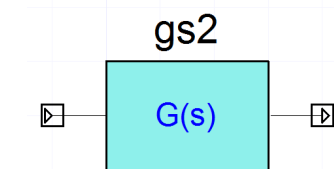
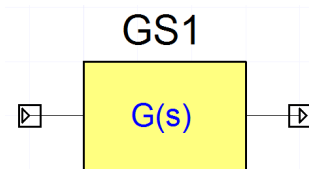
- Simulator immanent
- Sequentially processed
- Open integration
- Mind block sort order
- Solution after ECM , time delay
- No error minimization
- Hmax used, when no ECM and no fixed timestep given
- Typical for discrete-time operation

- Written in VHDL-AMS
- Closed solution within MNA (Modified Nodal Analysis)
- Closed integration
- No block sort order
- Solution with ECM, no time delay
- Error minimization from ECM
- Hmin important (timestep handling with ECM)
- Typical for arbitrary transfer functions

Transfer Function

- Example: representation of the following Transfer Function $G(s)$ for both yellow and blue block:

$$G(s) = \frac{100s^2 + 5s + 1}{50s^3 + 25s^2 + 10s + 3}$$



Parameters - GS1 - S-Transfer Function

Name: GS1 ☒ Show Name

Input Signal: 0 ☒ Use Pin

Numerator

Order: 2

Coefficient	Value
B[0]	1
B[1]	5
B[2]	100

Denominator

Order: 3

Coefficient	Value
A[0]	3
A[1]	10
A[2]	25
A[3]	50

Sample Time: ☒ Use System Sample Time

0 s ☐ Use Pin

Outputs

☒ Block Output Signal

OK Cancel

The right numerator and denominator polynomial order needs to be set first. The number of coefficients is automatically updated

Parameters - gs2 - S-Transfer Function Block in VHDL-AMS

Name: gs2 ☒ Show Name

Input Signal: 0 ☒ Use Pin

Numerator

Order: 2

Coefficient	Value
num[0]	1
num[1]	5
num[2]	100

Denominator

Order: 3

Coefficient	Value
den[0]	3
den[1]	10
den[2]	25
den[3]	50

Sample Time: ☒ Use System Sample Time

0 ☐ Use Pin

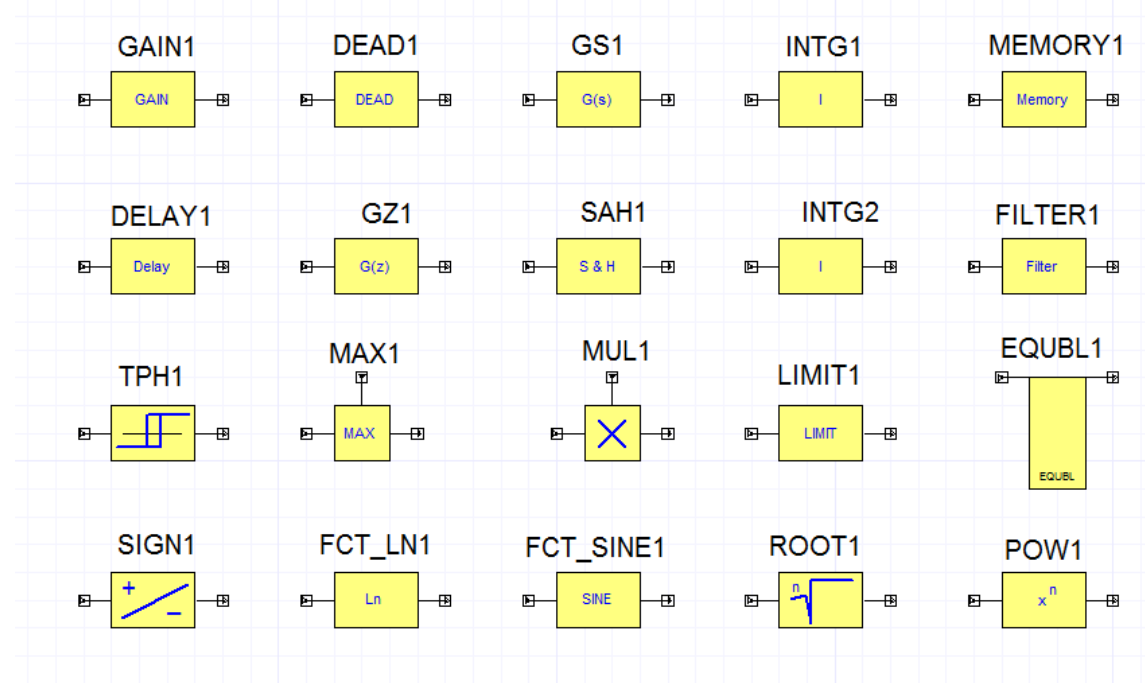
Outputs

☐ Block Output Signal

OK Cancel

Transfer Function and Blocks in SML

- Blocks
 - Continuous Blocks
 - DEAD: Dead Time
 - DIFF: Derivative
 - GAIN: Gain
 - GS: S-Transfer Function
 - INTG: Integrator
 - MEMORY: Memory
 - Discrete Blocks
 - DELAY: Delay
 - FILTER: Digital Filter
 - GZ: Z-Transfer Function
 - INTG: Discrete Integrator
 - SAH: Sample & Hold
 - UNITDELAY: Unit Delay
 - Sources Blocks
 - CONST: Constant Value
 - RANDOM: Random Value
 - STEP: Step Function
 - Signal Processing Blocks
 - COMP: Comparator
 - DIS: Discretization Element
 - EQUBL: Equation Block
 - LIMIT: Limiter
 - MAX: Maximum Input
 - MIN: Minimum Input
 - MINMAXT: Maximum & Minimum Value at Time T
 - MUL: Multiplier
 - NDNL: Multi dimensional table block
 - NEG: Negator
 - NL: Nonlinear Characteristic
 - NP: N-Point Element
 - SUM: Summation
 - TPH: Two-Point Element with Hysteresis
 - Math Blocks
 - FCT_ABS: Absolute Value
 - FCT_ARCCOS: Arccosine
 - FCT_COS: Cosine
 - FCT_EXP: Exponential Function
 - FCT_LN: Natural Logarithm
 - FCT_REC: Reciprocal Value
 - FCT_SINE: Sine
 - FCT_SINHYP: Sine Hyperbolic
 - FCT_TAN: Tangent
 - MOV_AV: Moving Average
 - POW: Power
 - ROOT: Root
 - SENSITIVITY: Sensitivity
 - SIGN: Sign



Continuous

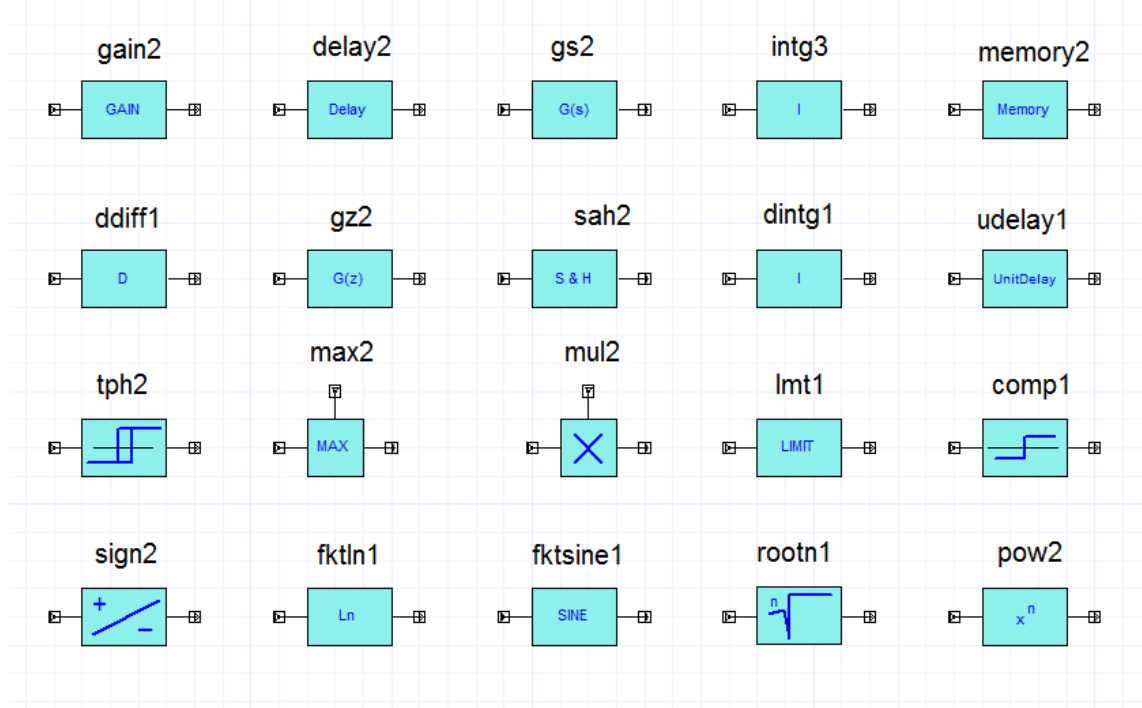
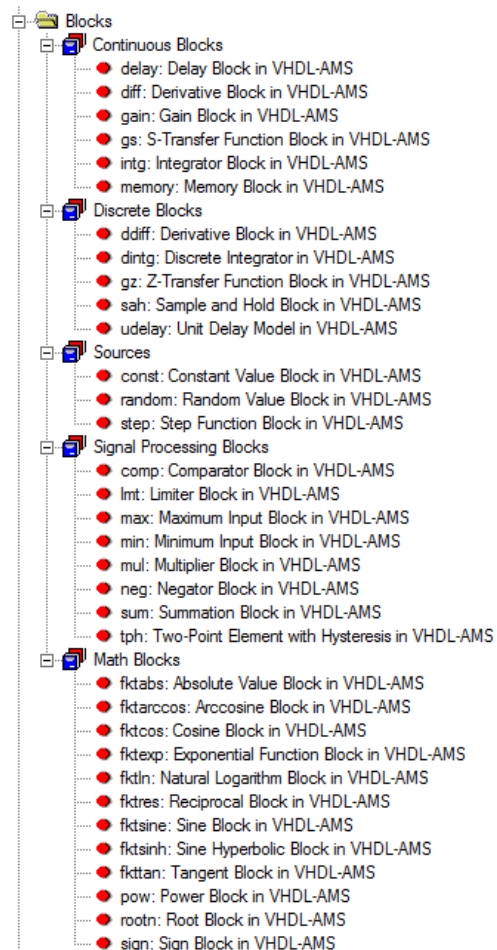
Discrete

Signal Processing

Math

– Examples of Blocks available in the default SML libraries

Transfer Function and Blocks in VHDL-AMS



Continuous

Discrete

Signal Processing

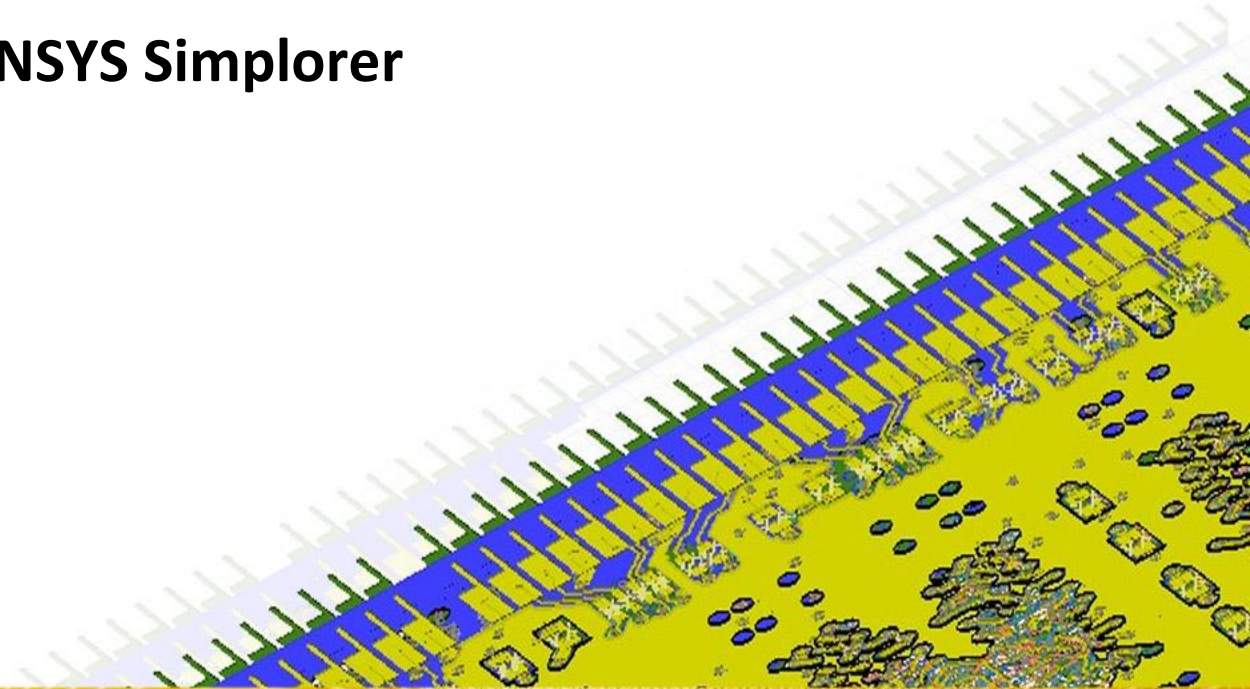
Math

- **Examples of Blocks available in the default VHDL-AMS libraries**
- **In addition, users can build their own blocks programming them in VHDL-AMS and/or in C++**



Post-Processing II

Introduction to ANSYS Simplorer



Report Plots

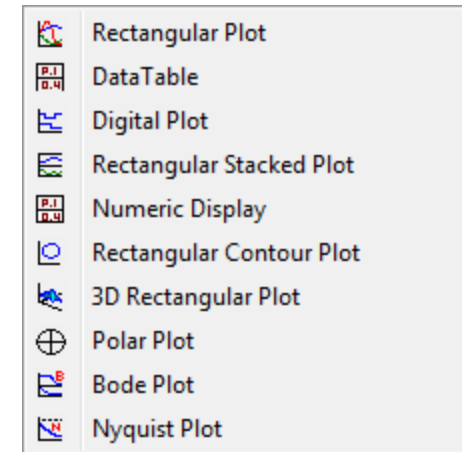
- Report Plots

- Report plots are used to analyze output quantities vs any defined parameter such as Time (transient analysis) or Frequency (AC analysis)
- Can be created from menu item *Draw* → *Report* → *<Plot Type>*

- Report Types

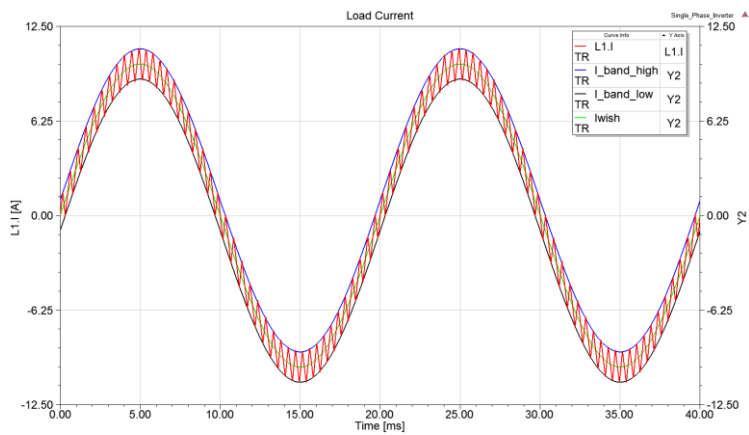
- Solver Specific Reports

- Plots for user-chosen specific quantities such as currents, voltages, assigned parameters etc.
 - Together with the usual Rectangular Plots, Simplorer offers a set of dedicated Plots like Bode, Nyquist, Polar Plots, etc.
 - In the following slides examples of the most used plots are shown

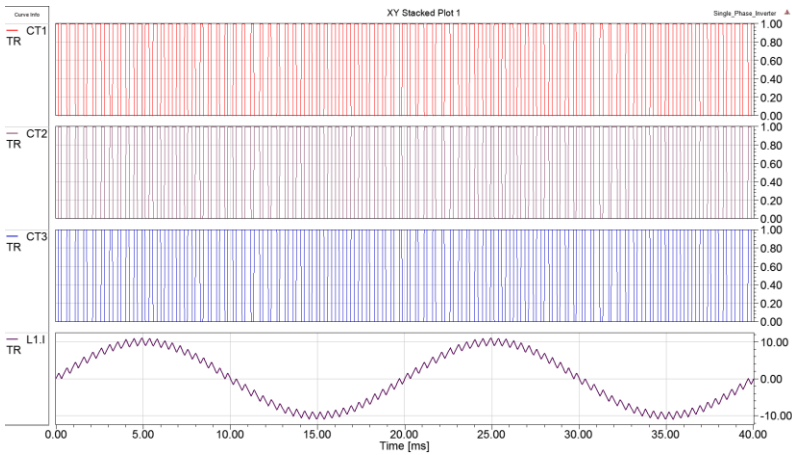


Report Plots

- Plots Types



Rectangular Plot:
Plots multiple traces overlaid in single Plot area



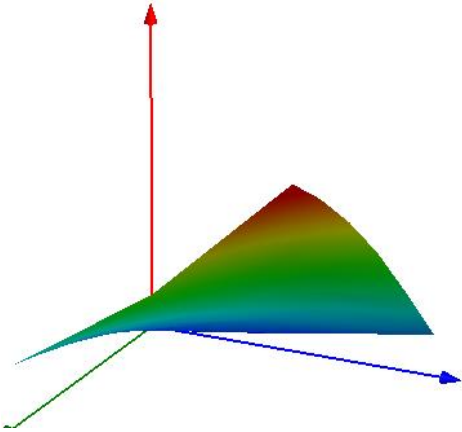
Rectangular Stacked Plot:
Plots multiple traces stacked vertically

Data Table 1

Single_Phase_Inverter

	Time [ms]	L1.I [A] TR	CT1 TR	CT2 TR	CT3 TR	CT4 TR
1	0.000000	-0.000000	1.000000	0.000000	0.000000	1.000000
2	0.010000	0.049175	1.000000	0.000000	0.000000	1.000000
3	0.020000	0.147428	1.000000	0.000000	0.000000	1.000000
4	0.030000	0.245682	1.000000	0.000000	0.000000	1.000000
5	0.040000	0.343886	1.000000	0.000000	0.000000	1.000000
6	0.050000	0.441693	1.000000	0.000000	0.000000	1.000000
7	0.060000	0.539601	1.000000	0.000000	0.000000	1.000000
8	0.070000	0.637412	1.000000	0.000000	0.000000	1.000000
9	0.080000	0.735124	1.000000	0.000000	0.000000	1.000000
10	0.090000	0.832738	1.000000	0.000000	0.000000	1.000000
11	0.100000	0.930255	1.000000	0.000000	0.000000	1.000000
12	0.110000	1.027674	1.000000	0.000000	0.000000	1.000000
13	0.120000	1.124996	1.000000	0.000000	0.000000	1.000000
14	0.130000	1.222220	1.000000	0.000000	0.000000	1.000000
15	0.140000	1.319346	1.000000	0.000000	0.000000	1.000000
16	0.150000	1.416376	1.000000	0.000000	0.000000	1.000000
17	0.160000	1.513308	0.000000	1.000000	1.000000	0.000000
18	0.170000	1.510193	0.000000	1.000000	1.000000	0.000000
19	0.180000	1.407183	0.000000	1.000000	1.000000	0.000000
20	0.190000	1.304276	0.000000	1.000000	1.000000	0.000000
21	0.200000	1.201421	0.000000	1.000000	1.000000	0.000000

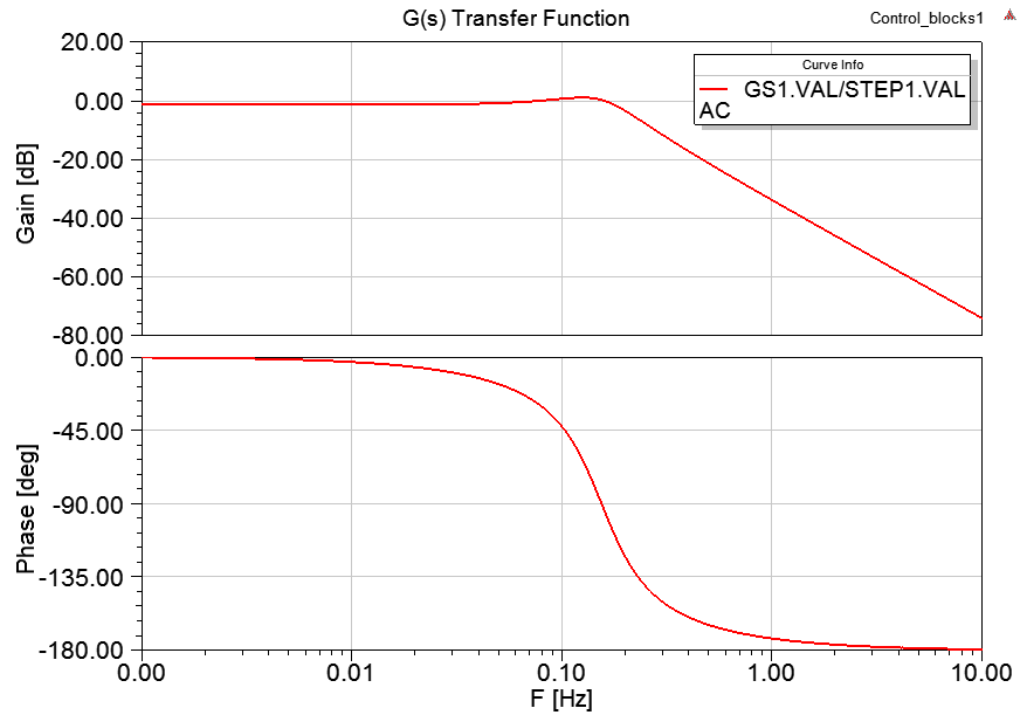
Data Table:
Plots traces in tabular form



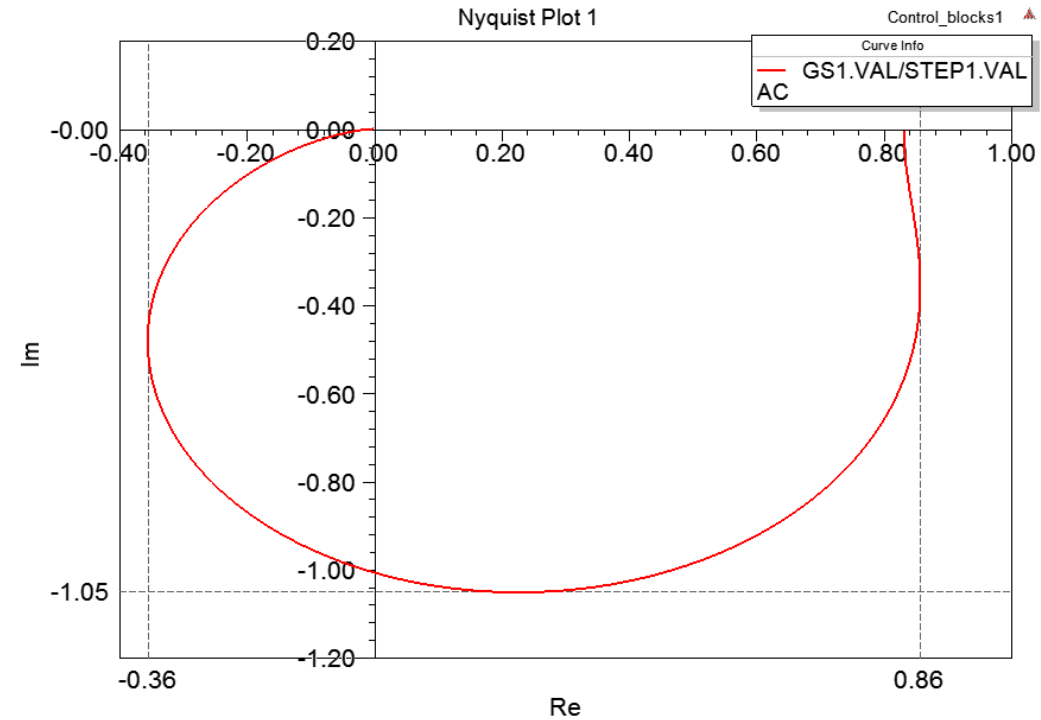
3D Rectangular Plot:
Plots 3D surface of output against two inputs

Report Plots

- Plots Types



Bode Plot: Plots magnitude (dB) and phase of a signal (ratio between two quantities) vs Frequency into two separated graphs in the same plot area



Nyquist Plot: Plots the imaginary part of a signal (ratio between two quantities) vs the real part while the frequency changes

Report Plots

- **Creating Rectangular Plot**

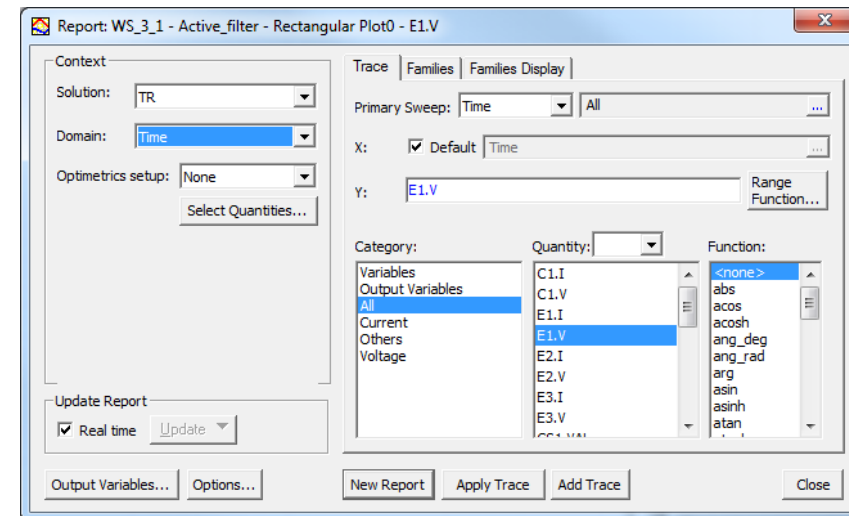
- Can be created from menu item *Draw* → *Report* → *Rectangular Plot*

- **Context**

- **Solution:** choose from available solution types (TR, AC, DC)
 - **Domain:** if TR is selected, choose between Time and Spectral. If AC is checked, Domain is only sweep
 - **Optimetrics Setup:** if present, select the available optimetric analysis

- **Trace Tab**

- **Primary Sweep:** controls the independent variable
 - **X:** controls any functional operator on the independent variable (set to Primary Sweep)
 - **Y:** select the value to be plotted
 - **Category:** Select the variable category
 - **Quantity:** Select the variable to plot
 - **Function:** To perform arithmetic operations on variable before plot



Report Plots

– Families Tab

- Enables users to plot Separate Traces for each variable value from defined parametric sweep

– Output Variables

- Opens Output variable definition window

– New Report

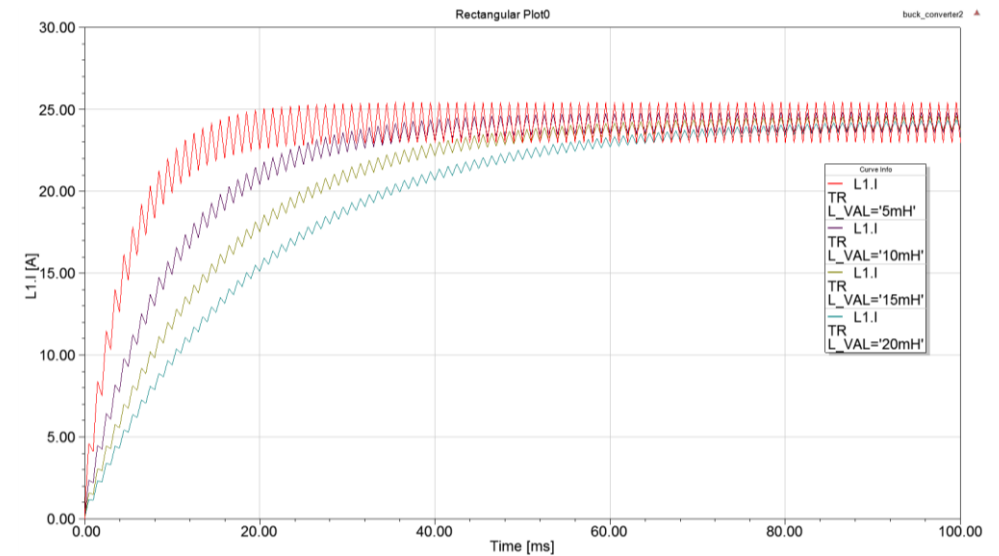
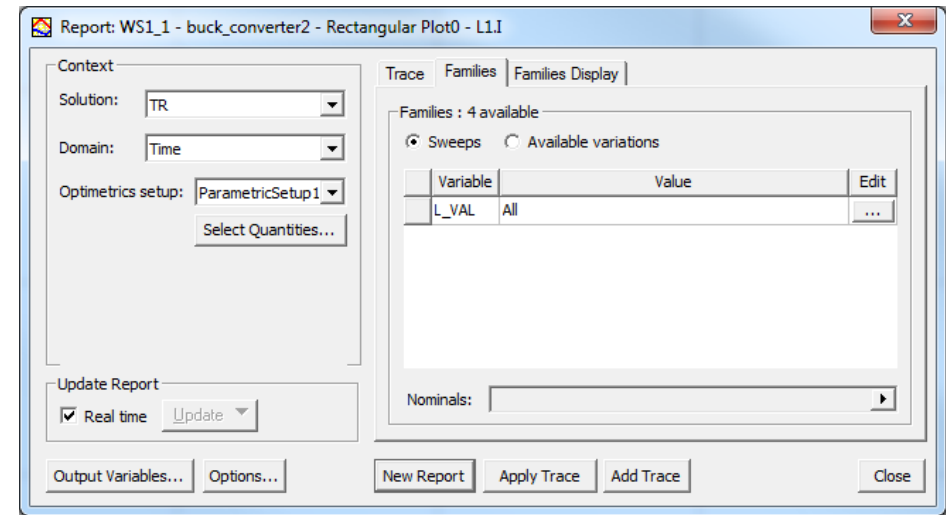
- Creates a New XY Plot

– Add Trace

- Adds defined trace to selected XY Plot

– Apply Trace

- Replaces existing trace with selected one



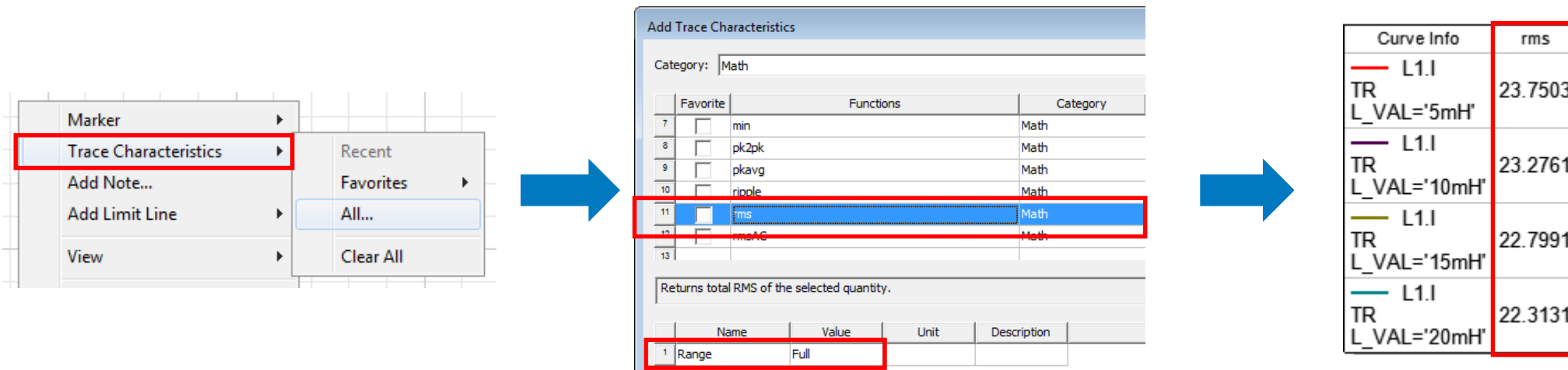
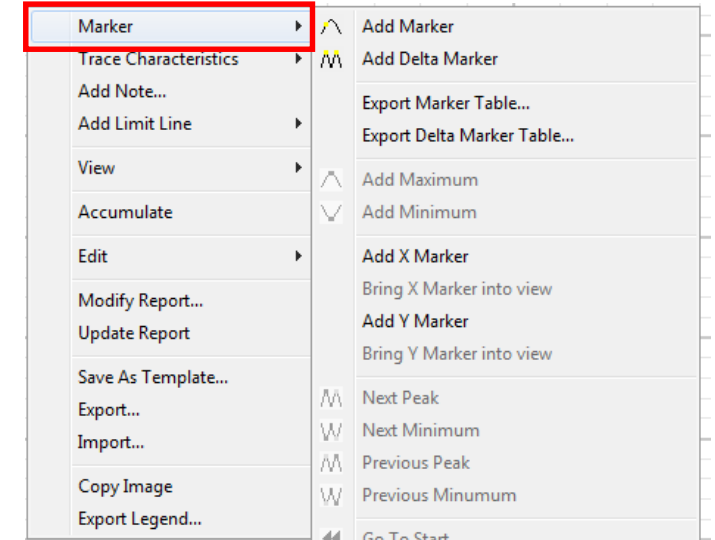
Report Analysis

- **Markers**

- Markers help to analyze the plot data at various data points
- Can be used to get the value of outputs at any input point, identify change in output over a range or get the slope of the curve between two points
- Can be added by RMB on Report Plot area and selecting **Marker**

- **Trace Characteristics**

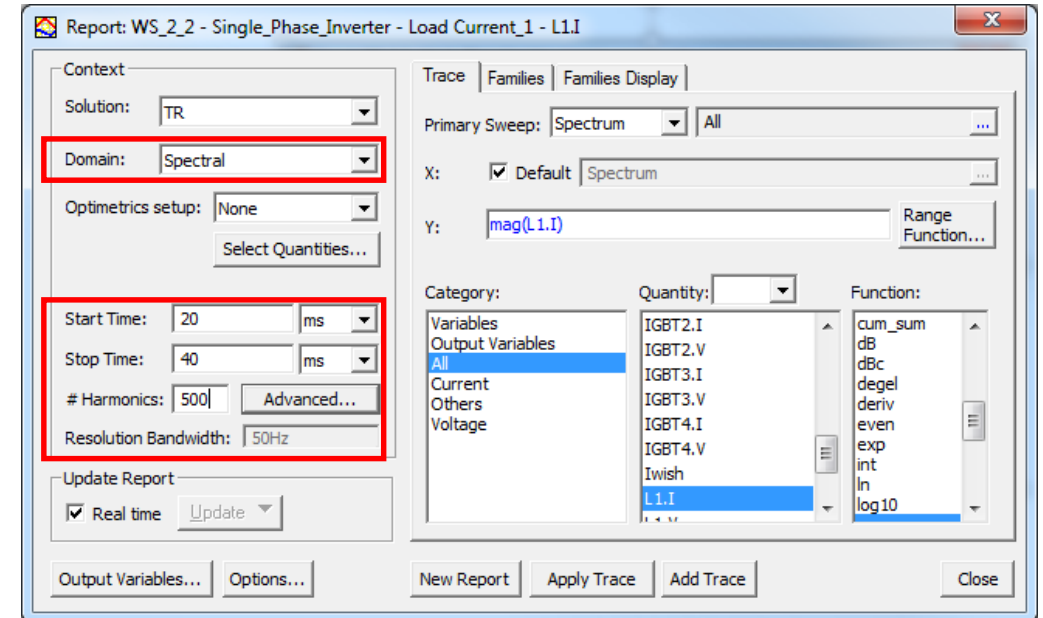
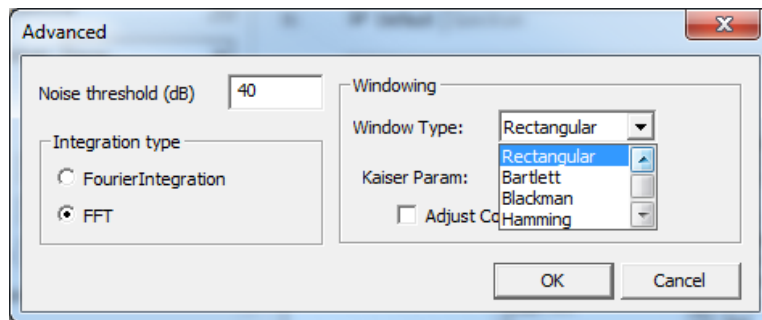
- Trace Characteristics enable users to calculate signal characteristics on the plotted traces
- Resulting value is displayed next to the trace



Report Analysis

- Spectral Analysis

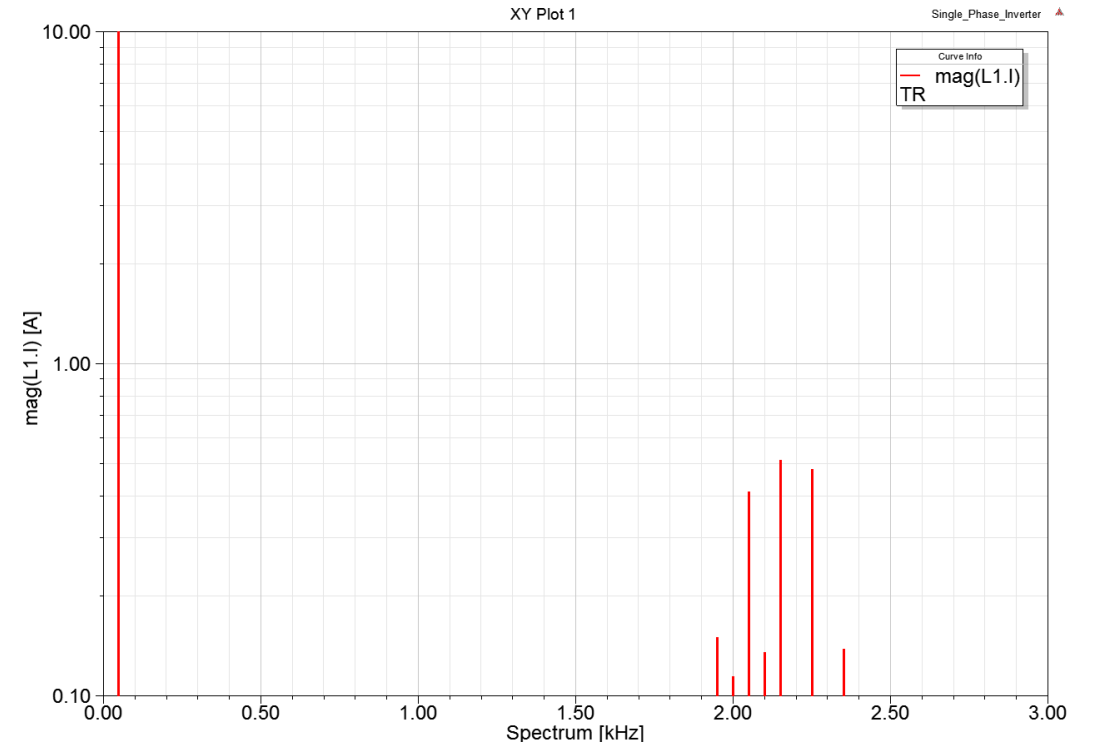
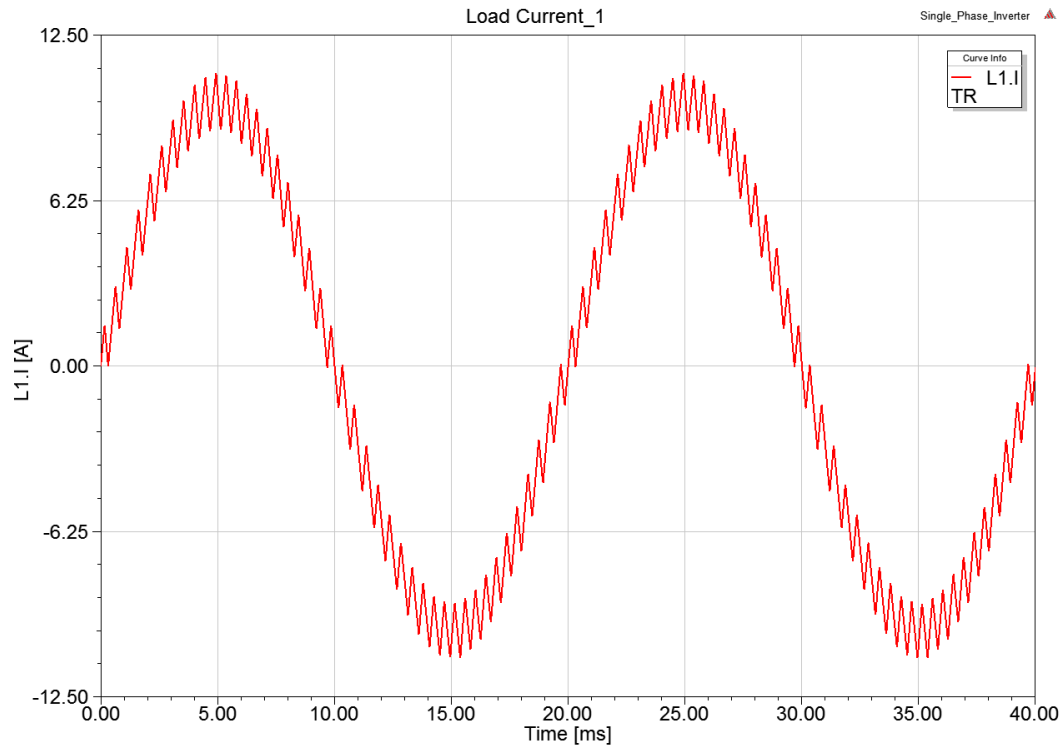
- For TR analysis, if **Spectral** Domain is chosen, further settings appear, allowing user to define the FFT (Fast Fourier Transform) parameters analysis:
 - **Start Time**: define the initial time used for FFT
 - **Stop time**: define the final time used for FFT
 - **# Harmonics**: this parameter affects the accuracy and should be set around 500 - 1000
 - **Advanced**: allows users to set the **threshold noise**, to perform the normal (usually very long) **Fourier Integration** in place of FFT, and/or change the window type from Rectangular (default) to Bartlett, Hamming, etc.



Report Analysis

- Spectral Analysis

- Example of function in time domain transformed through the FFT:

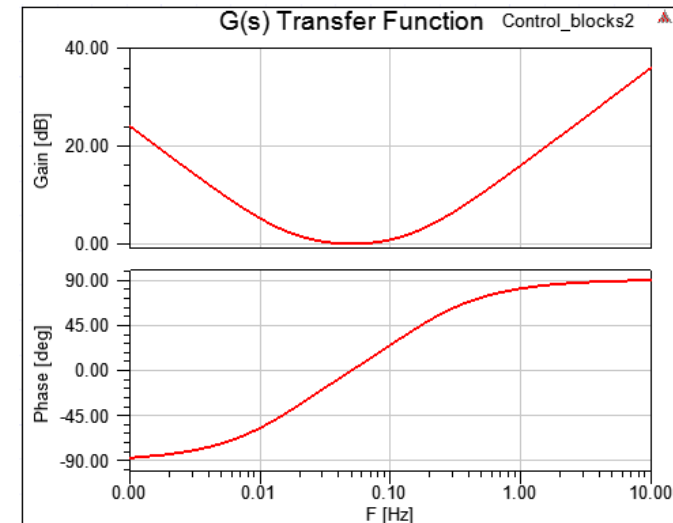
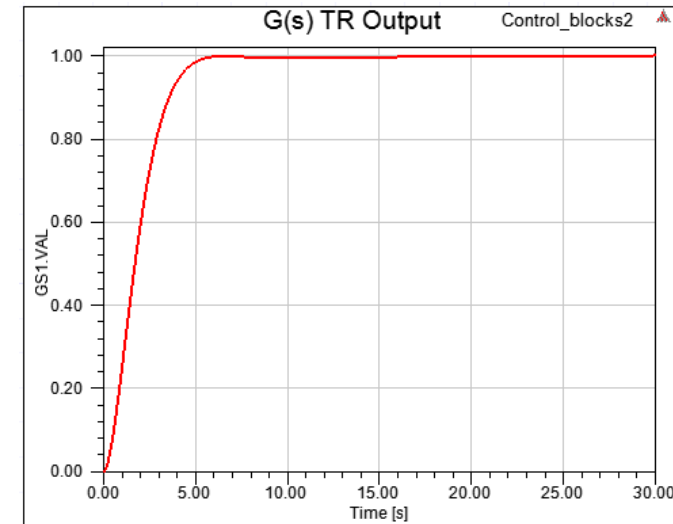
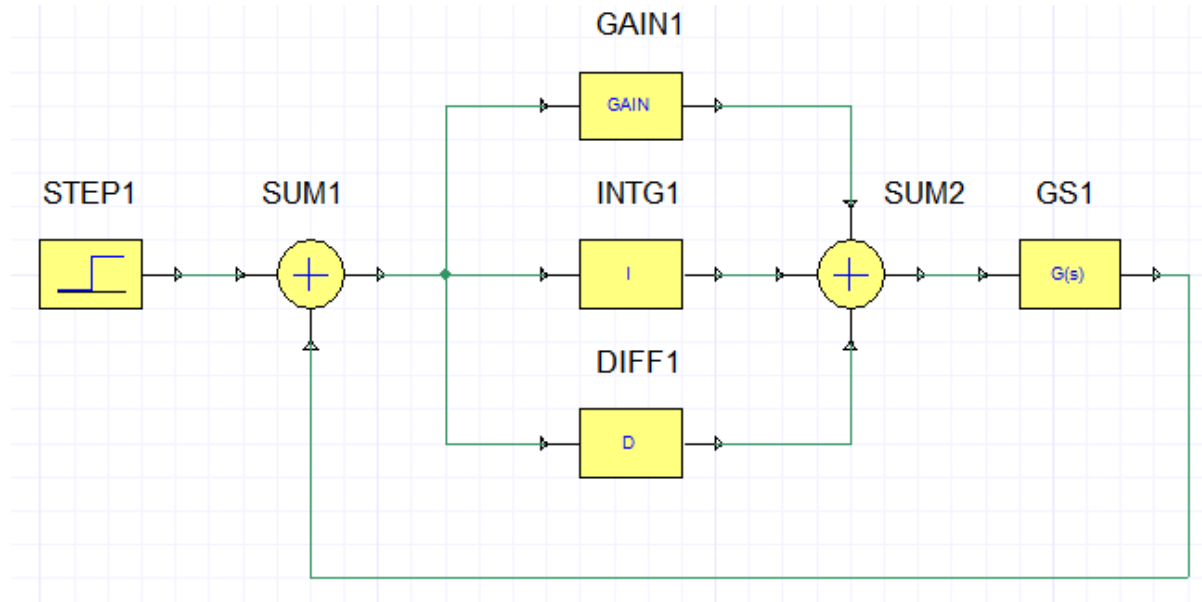


Summary

What have we learned in this session?

- **Sub-circuits**
 - How to create a sub-circuit
 - Port-components
- **Transfer Functions and blocks**
 - G(s) Block
 - Differences between yellow (SML) and blue (VHDL-AMS) blocks
 - Overview on the default blocks
- **Post-Processing II**

Workshop 3.1 – Transfer Function and Control Blocks



Workshop 3.2 – Sub-Circuits

