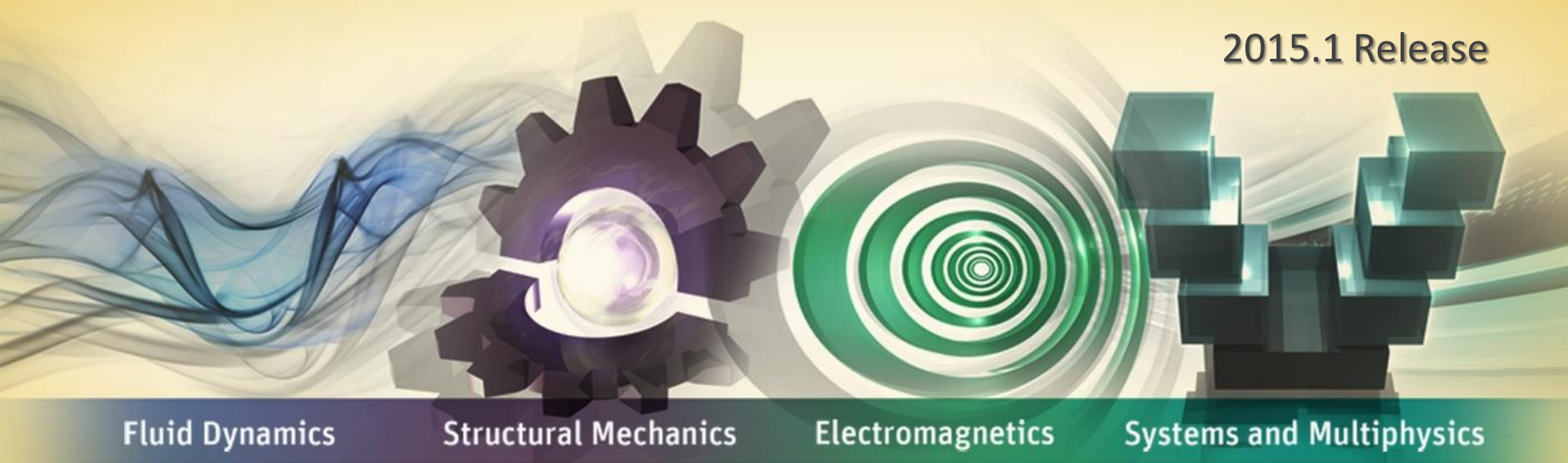


Workshop 1-1: Resonant Modes

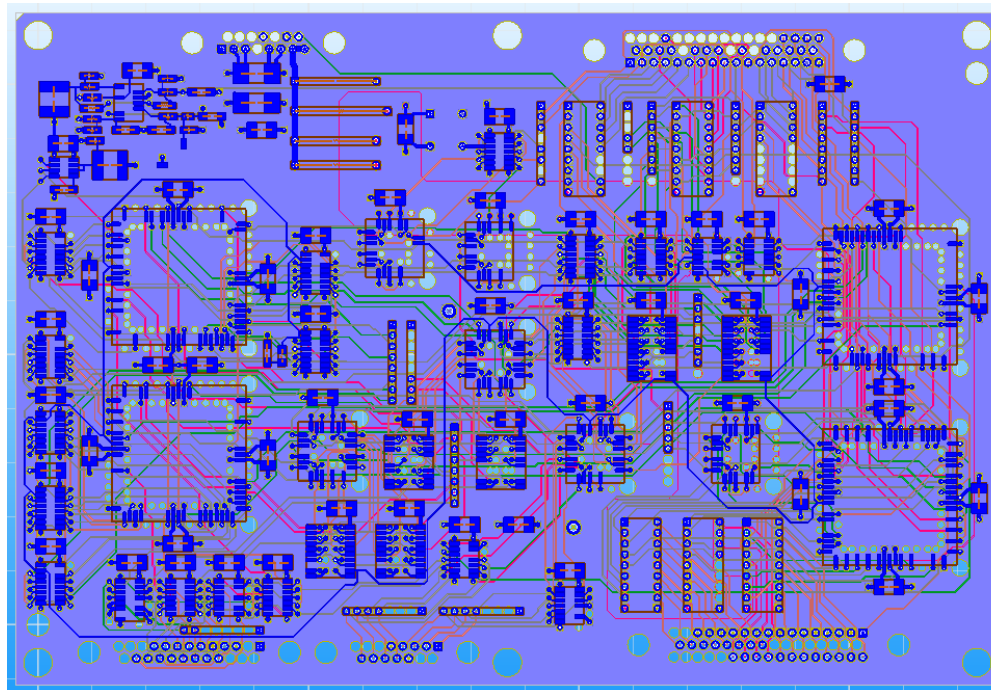
2015.1 Release



Introduction to ANSYS SIwave

- **Board Design**

- The board design example is intended to show you how to import , simulate, and analyze a 4-layer board structure using SIwave.
- When traces are routed through power and ground planes, you can experience signal integrity problems. The following illustration details the board design that will be used in SIwave to investigate the following SI applications:
 - How resonant behavior effects signal transmission along a trace
 - Non-ideal plane behavior
- For this example, we will import the design file and its discrete components. After defining the correct capacitance, ESL, and ESR values, a resonant mode calculation will be performed. We will then add decoupling capacitors to the planes to see if an improvement can be made in the resonant mode voltage swing.



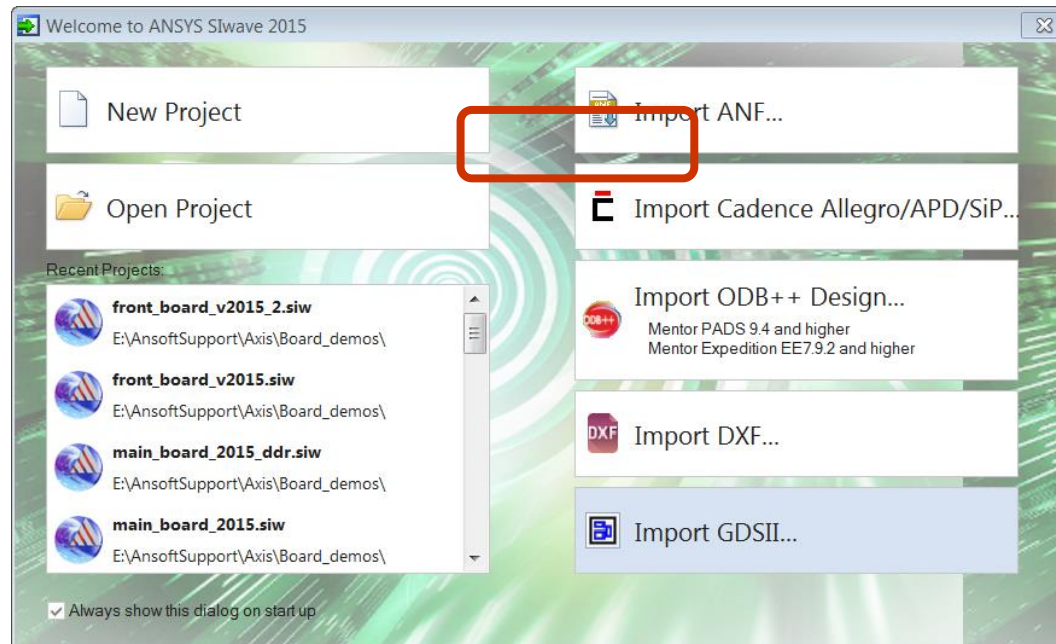
- **ANSYS Siwave Design Environment**

- The following features of the ANSYS Siwave Design Environment are used to create this passive device model
 - **Importing**
 - ANF file
 - Component File
 - **Editing Component Values**
 - Capacitance
 - ESL
 - ESR
 - **Adding Components**
 - Ports
 - **Solutions**
 - Resonant Modes
 - S-Parameters
 - Full Wave Spice Sub-circuit
 - **Fields**
 - Resonant Mode Plot
 - **Plots**
 - S-Parameter sweep

Example – Board Design

• Starting SIwave

- To launch SIwave, click the Microsoft **Start** Button, select: **All Programs > ANSYS Electromagnetics > ANSYS Electromagnetics Suite 16.1 > ANSYS SIwave 2015.1**
 - The Welcome Window will appear

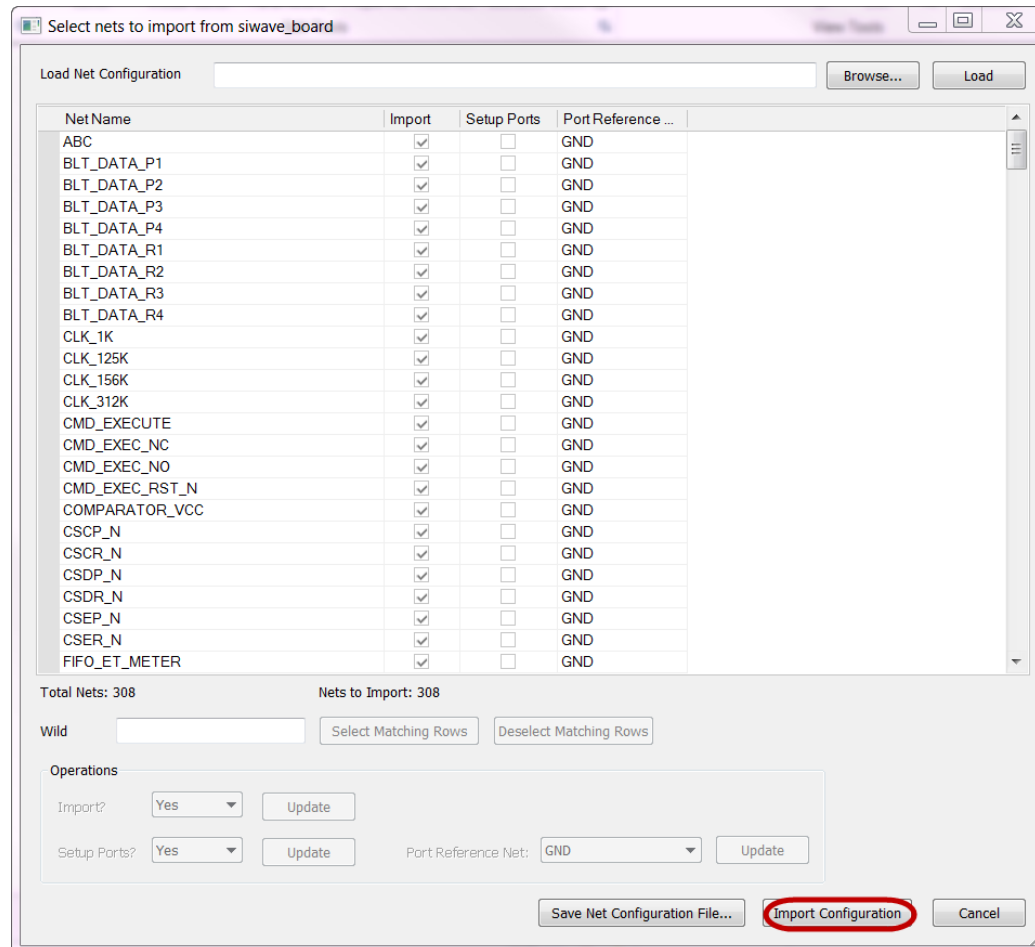


• Import the .ANF (Ansoft Neutral File) file

- Click the Import ANF... box
 - Navigate to the file named: **siwave_board.anf**
 - Click the **Open** button

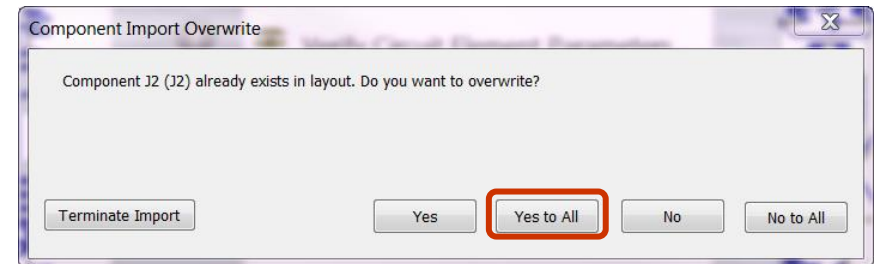
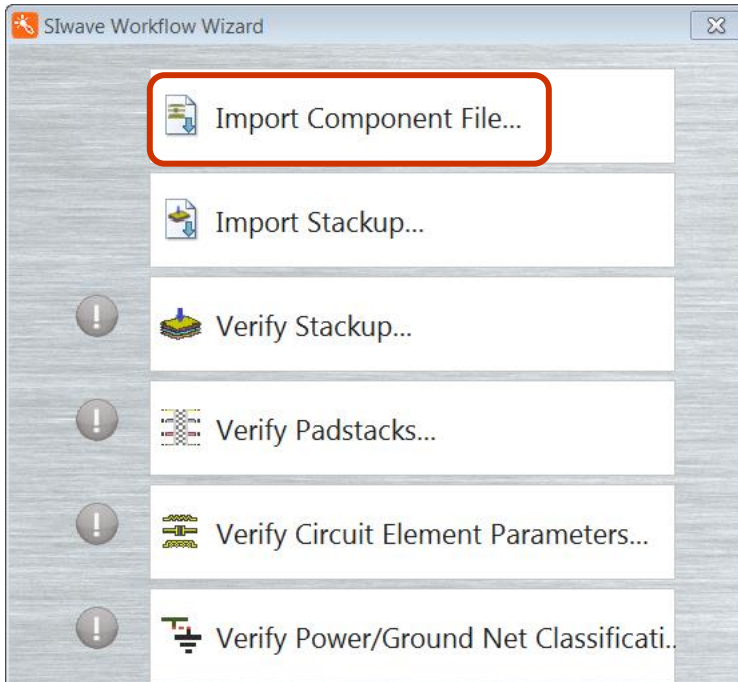
Example – Board Design

- The Select nets box will appear. (If desired, the user can filter nets to be imported. For this example, all nets will be imported)
- Click the **Import Configuration** button



Example – Board Design

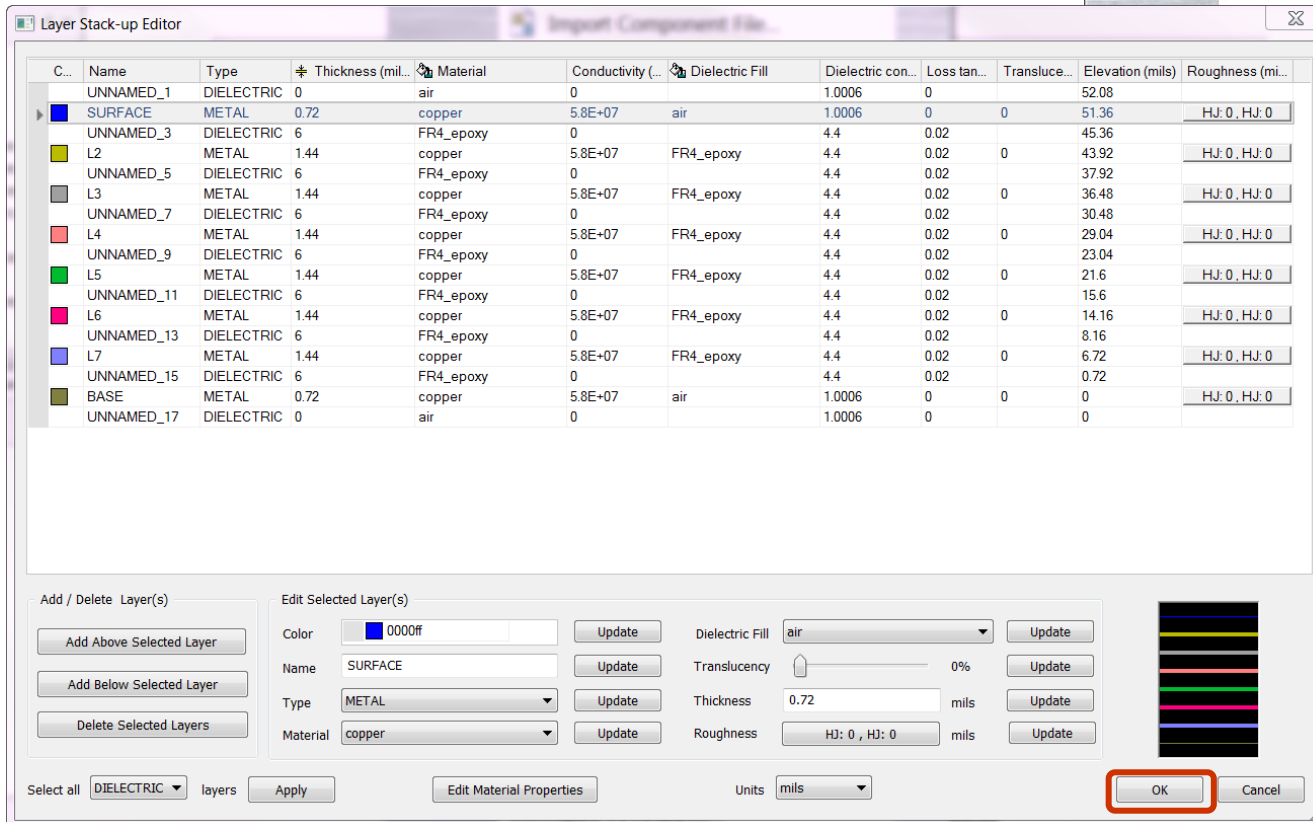
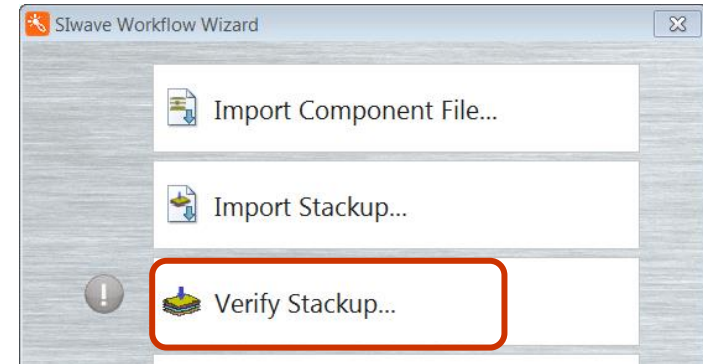
- The SIwave Workflow Wizard will appear
- Import the .CMP (Ansoft Component File)
 - Click on the Import Component File button
 - Navigate to the file named: **siwave_board.cmp**
 - Click the **Open** button
 - If there is a warning message click the **Yes to All** button to overwrite existing names



Example – Board Design

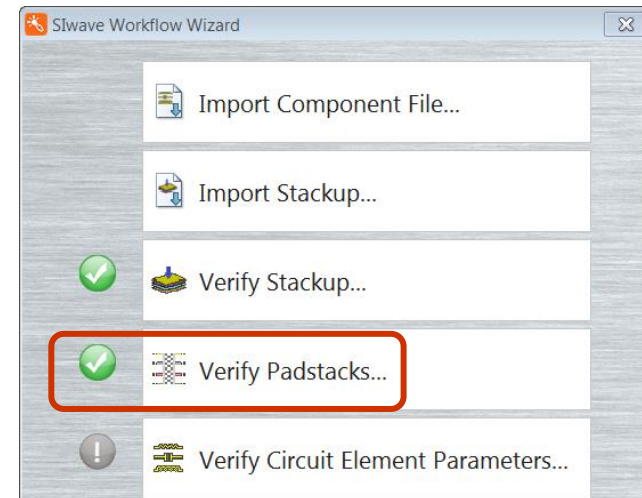
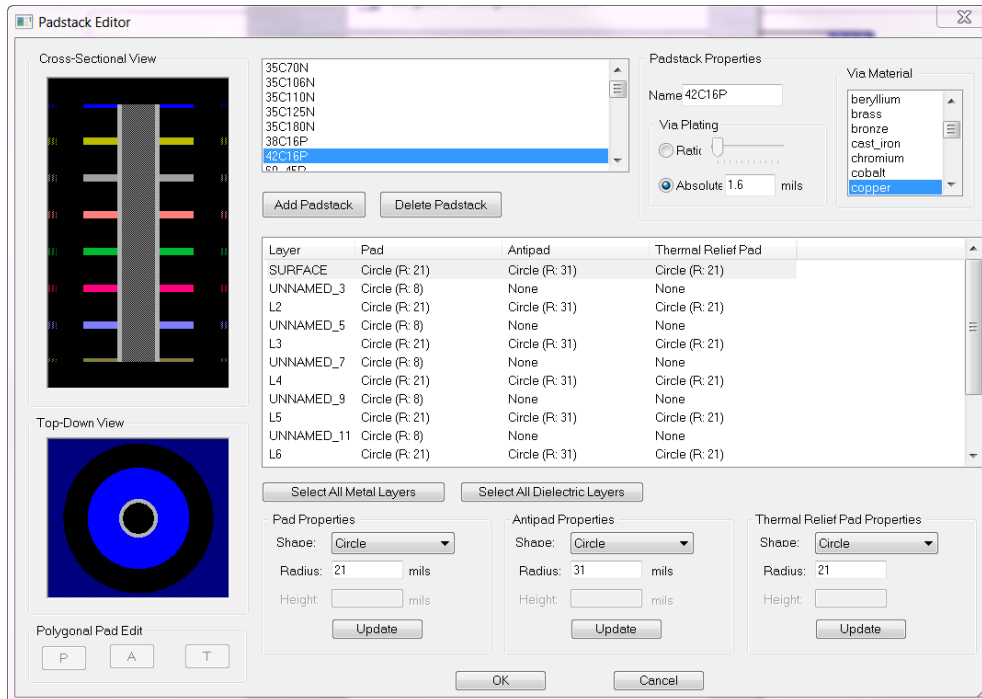
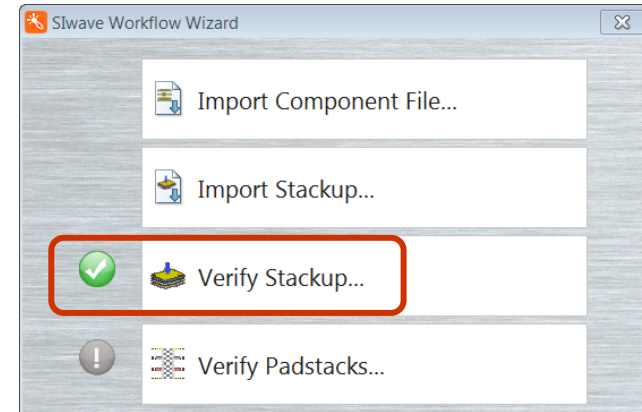
• Verify the Layer Stackup

- From the SIwave Workflow Wizard dialog, click Verify Stackup...
- Double-check the values with those shown in the table below
- Click OK when finished



Example – Board Design

- **Verify the Layer Stackup**
 - There should be a green check mark next the to Verify Stackup
- **Verify Padstacks**
 - Click on Verify Padstacks to view
 - View some of the Padstacks
 - Click OK when finished
 - There should be a green check mark next to Verify Padstacks



Example – Board Design

• Verify and Reassign Circuit Element Parameters

- Click on Verify Circuit Element Parameters
 - Click on the Capacitors Tab to verify that there are 64 capacitors
 - Click on the Inductors Tab to verify that there is 1 inductor
 - Click on the Resistors Tab to verify that there are 16 resistors
 - Click OK when finished
- Click on the X to close the SIwave Workflow Wizard

Circuit Element Properties

Capacitors Inductors Resistors Ports Voltage Probes Current Sources Voltage Sources Net Terminals

| ★ | Active | ∂/∂f | Part Number | RefDes | Capacitanc... | Parasitic ... | Parasitic R (...) | Positive "Terminal" Net | Negative " |
|---|--------|------|----------------------------|--------|---------------|---------------|-------------------|-------------------------|------------|
| ✓ | Yes | ✗ | CAPACITOR_CDR06 | C1 | 1E-07 | 0 | 0 | GND | UN4CAPA |
| ✓ | Yes | ✗ | CAPACITOR_CDR04 | C2 | 1E-07 | 0 | 0 | GND | VCC |
| ✓ | Yes | ✗ | CAPACITOR_CDR06 | C3 | 1E-07 | 0 | 0 | GND | UN105554F |
| ✓ | Yes | ✗ | CAPACITOR_CDR02 | C4 | 1E-07 | 0 | 0 | GND | UN4CAPA |
| ✓ | Yes | ✗ | CAPACITOR_CDR04 | C5 | 1E-07 | 0 | 0 | GND | COMPARA |
| ✓ | Yes | ✗ | CAPACITOR_CDR02 | C6 | 1E-07 | 0 | 0 | GND | UN4CAPA |
| ✓ | Yes | ✗ | CAPACITOR_CDR02 | C7 | 1E-07 | 0 | 0 | GND | POR_RST |
| ✓ | Yes | ✗ | CAPACITOR_CDR02 | C8 | 1E-07 | 0 | 0 | GND | UN4CAPA |
| ✓ | Yes | ✗ | CAPACITOR_CWR06-10V,47,10% | C9 | 1E-07 | 0 | 0 | GND | VCC |
| ✓ | Yes | ✗ | CAPACITOR_CWR06-10V,47,10% | C10 | 1E-07 | 0 | 0 | GND | VCC |
| ✓ | Yes | ✗ | CAPACITOR_CDR04 | C11 | 1E-07 | 0 | 0 | GND | VCC |
| ✓ | Yes | ✗ | CAPACITOR_CSR13B | C12 | 1E-07 | 1E-09 | 0.05 | GND | UN2CAPA |
| ✓ | Yes | ✗ | CAPACITOR_CDR04 | C13 | 1E-07 | 0 | 0 | GND | VCC |
| ✓ | Yes | ✗ | CAPACITOR_CDR04 | C14 | 1E-07 | 0 | 0 | GND | VCC |
| ✓ | Yes | ✗ | CAPACITOR_CDR04 | C15 | 1E-07 | 0 | 0 | GND | VCC |
| ✓ | Yes | ✗ | CAPACITOR_CDR02 | C16 | 1E-07 | 0 | 0 | GND | UN105554F |
| ✓ | Yes | ✗ | CAPACITOR_CDR04 | C17 | 1E-07 | 0 | 0 | GND | VCC |
| ✓ | Yes | ✗ | CAPACITOR_CDR04 | C18 | 1E-07 | 0 | 0 | GND | VCC |

64 capacitors, 64 active, 0 inactive

Modify Properties...

Modify Layers...

Delete

Fit Selection

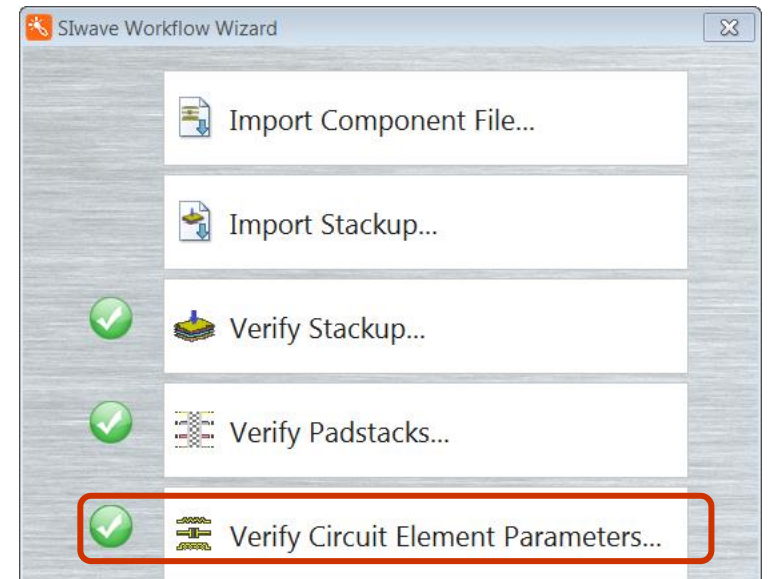
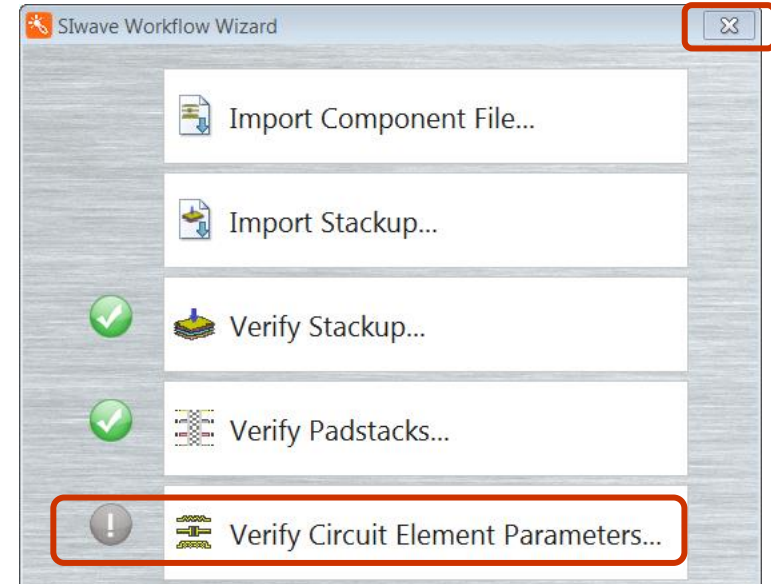
Activate

Deactivate

Export

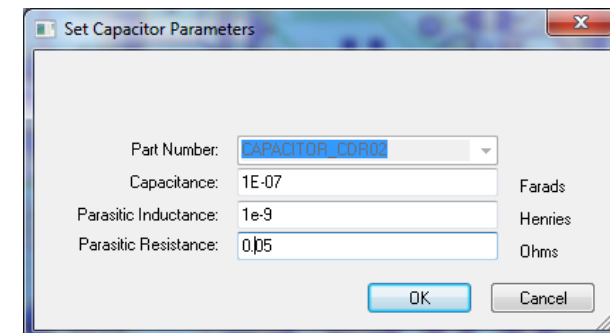
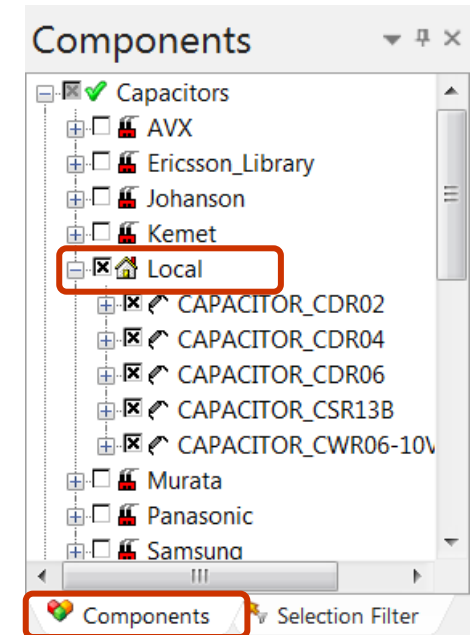
OK

Cancel



• Editing the Capacitance Values

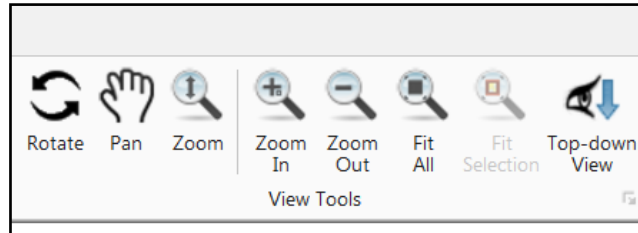
- Select the **Components** tab
 - Expand **Capacitors** by clicking the plus sign next to it
 - Expand **Local** by clicking the plus sign next to it
 - Highlight **CAPACITOR_CDR02**
 - Right click **CAPACITOR_CDR02** and select **Edit Component Properties**
 - Capacitance: **1E-7**
 - Parasitic Inductance: **1E-9**
 - Parasitic Resistance: **0.05**
 - Click the **OK** button
 - Highlight **CAPACITOR_CDR04**
 - Right click **CAPACITOR_CDR04** and select **Edit Component Properties**
 - Capacitance: **1E-7**
 - Parasitic Inductance: **1E-9**
 - Parasitic Resistance: **0.05**
 - Click the **OK** button
 - Highlight **CAPACITOR_CDR06**
 - Right click **CAPACITOR_CDR06** and select **Edit Component Properties**
 - Capacitance: **1E-7**
 - Parasitic Inductance: **1E-9**
 - Parasitic Resistance: **0.05**
 - Click the **OK** button



- **Editing the Capacitance Values (continued)**
 - Highlight **CAPACITOR_CSR13B**
 - Right click **CAPACITOR_CSR13B** and select **Edit Component Properties**
 - Capacitance: **1E-7**
 - Parasitic Inductance: **1E-9**
 - Parasitic Resistance: **0.05**
 - Click the **OK** button
 - Highlight **CAPACITOR_CWR06-10V,47,10%**
 - Right click **CAPACITOR_CWR06-10V,47,10%** and select **Edit Component Properties**
 - Capacitance: **4.7E-5**
 - Parasitic Inductance: **1E-8**
 - Parasitic Resistance: **0.5**
 - Click the **OK** button
- **Save the Design**
 - Select **File > Save**

- **Changing the View**

- From the HOME tab, the view menu can be accessed



- **Shortcuts**

- Since changing the view is a frequently used operation, some useful shortcut keys exist. Press the appropriate keys and drag the mouse with the left button pressed:

- **Rotate**

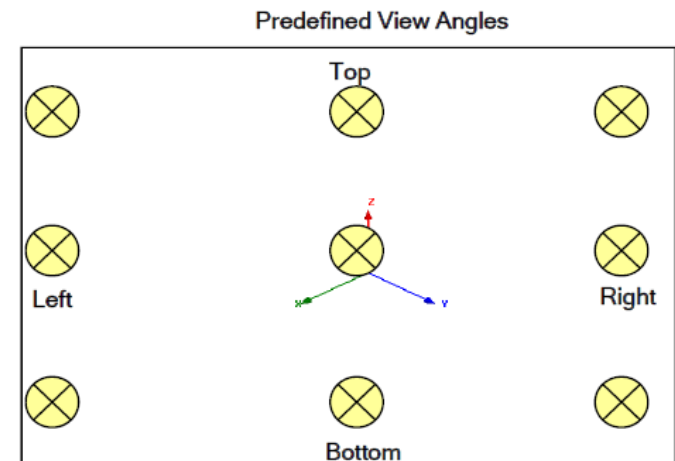
- **ALT + Drag** or press the roller button on the mouse
- In addition, there are 9 pre-defined view angles that can be selected by holding the ALT key and double clicking on the locations shown on the next page.

- **Pan**

- **Shift + Drag**

- **Dynamic Zoom**

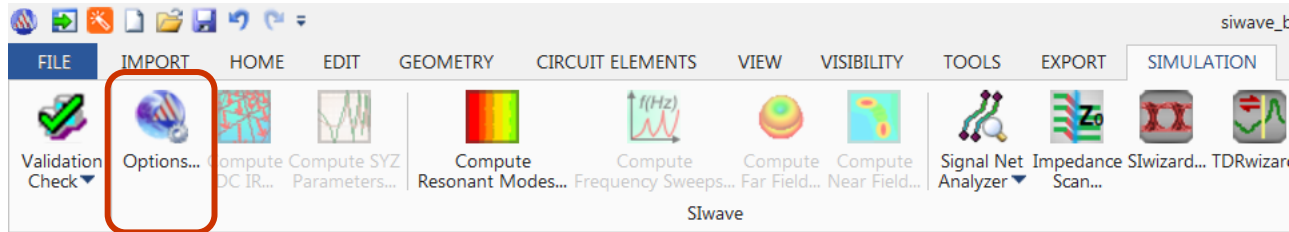
- **ALT + Shift + Drag** or use the roller on the mouse



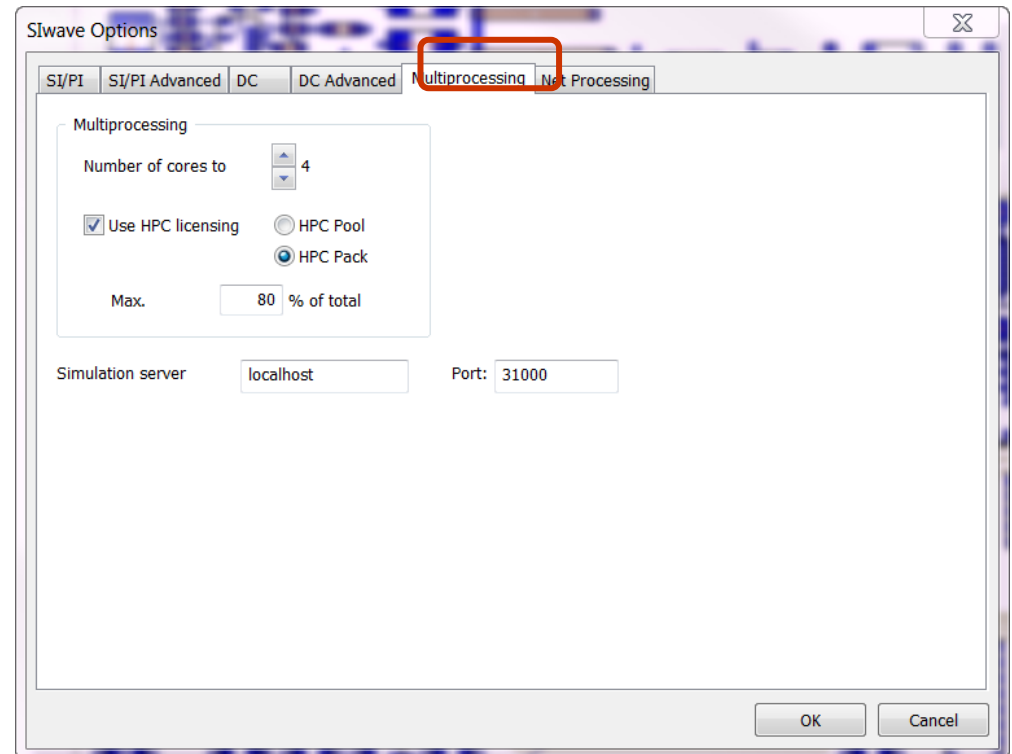
Example – Board Design

- **Setting Simulation Options**

- Click on the Simulation Tab to access the Options button



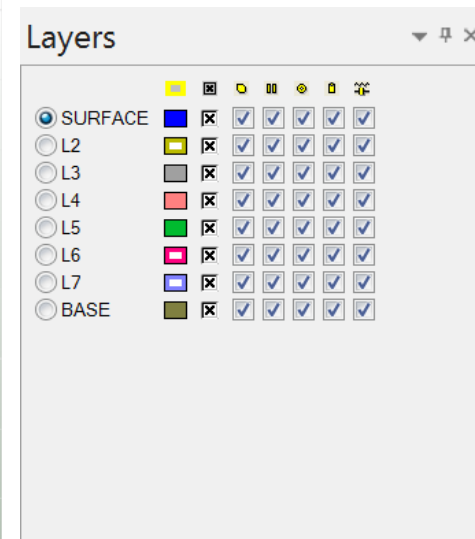
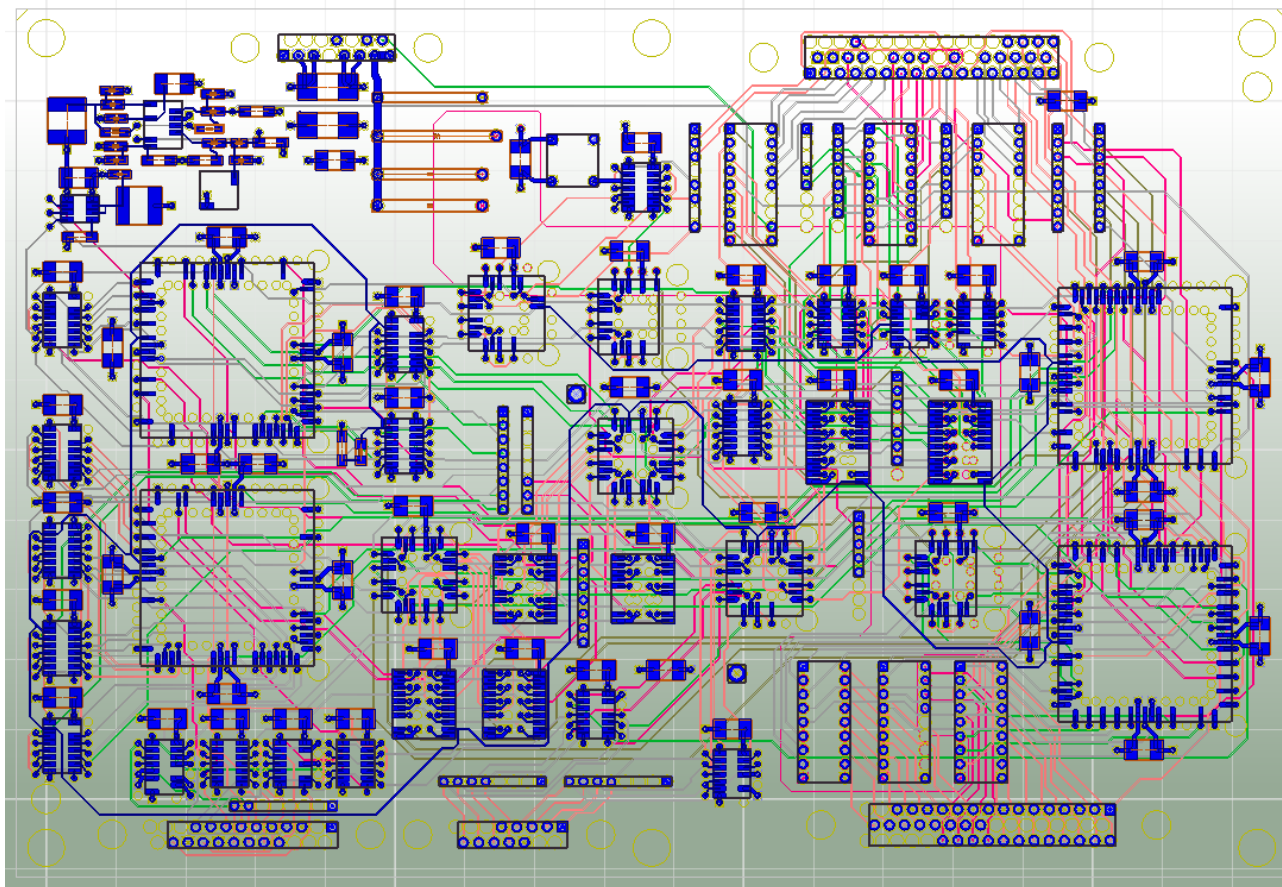
- Click on the Multiprocessing Tab
 - Number of cores to use: 4
 - Use HPC Licensing: checked, HPC Pack
 - Click OK



SIwave Resonant Mode Analysis

- **Set Visibility options**

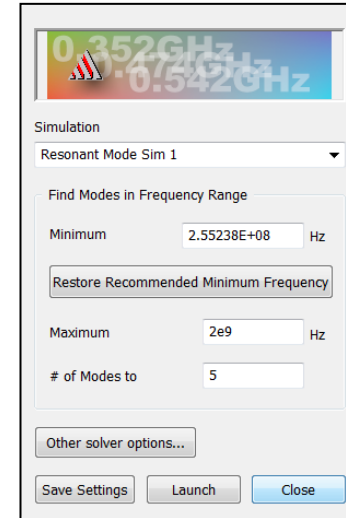
- Using the checkboxes in the Layers workspace, turn on full visibility of all layers
- Click the colored rectangles next to each layer name to control whether the geometry is shown in outline or filled form



Example – Board Design

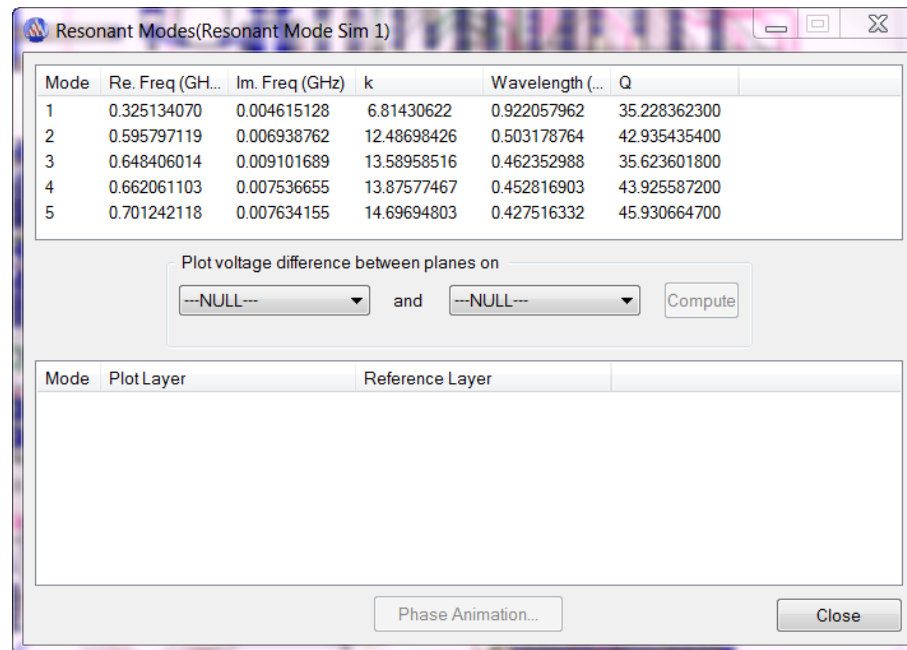
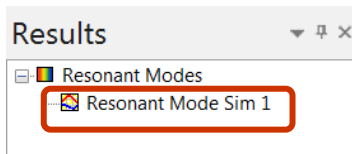
• Running a Resonant Mode Simulation

- From the Simulation Tab click the **Compute Resonant Modes** button
 - Simulation name: **Resonant Mode Sim 1**
 - Minimum Frequency: **2.55238E+008**
 - Maximum Frequency: **2e9**
 - # of Modes to Compute: **5**
 - Click the **Launch** button



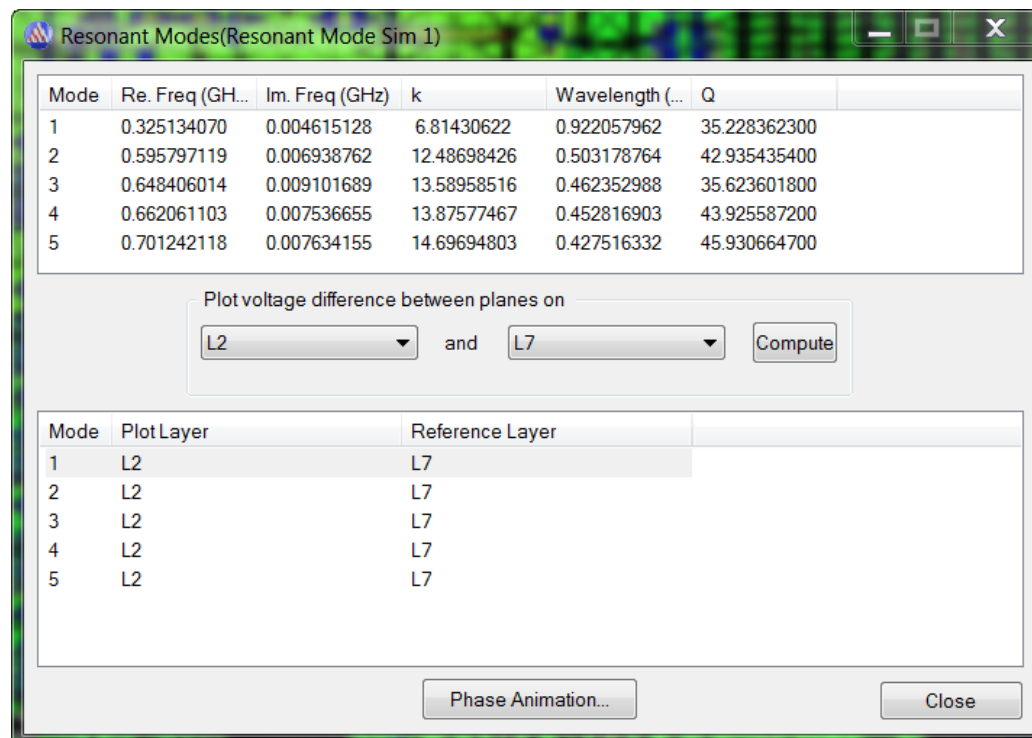
• Viewing Results

- Right-click on Resonant Mode Sim1
- Select View Results



• Viewing Results (continued)

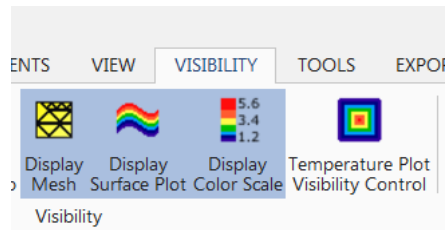
- The voltage difference between planes can be displayed for each resonant mode. It is the transverse (x,y) dependence of the voltage difference that will be plotted.
- Generate the voltage plot between planes **L2** and **L7** by selecting the layers as shown here and pressing **Compute**. This computation is required to generate the 2D plot from existing solution data.
- When the computation is done, the various voltage plots can be viewed for each mode by selecting the correct row in the bottom section of the Resonant Mode Results window.



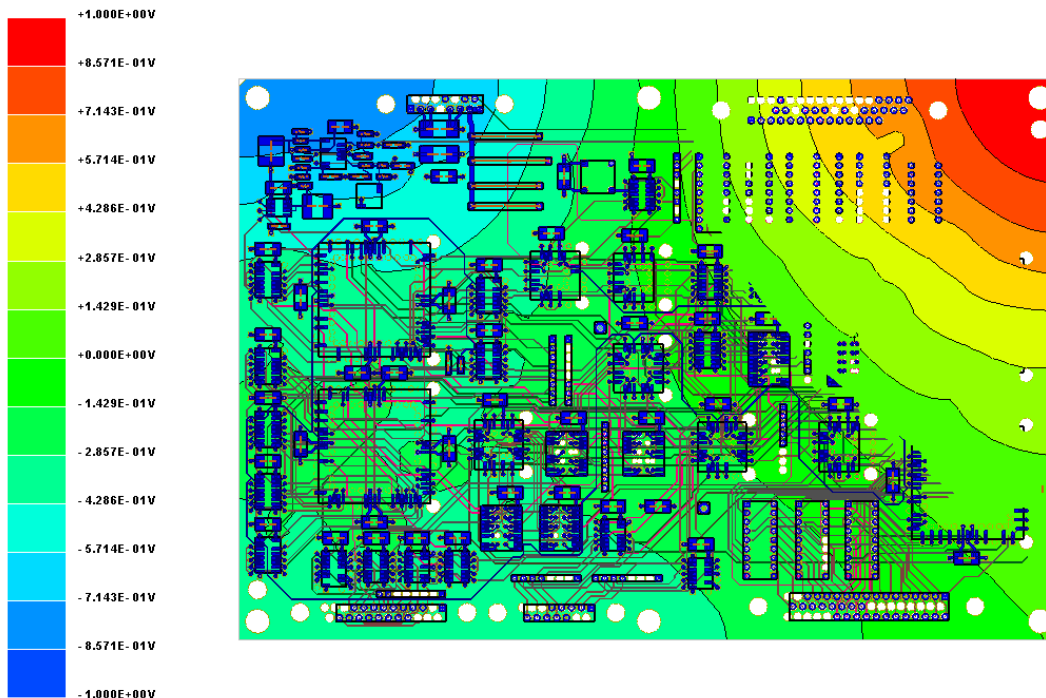
Example – Board Design

- **Viewing Results (continued)**

- While viewing the voltage distribution, the mesh and color-key visibility may be toggled from the Visibility window



- The voltage distribution of the 5th mode is shown here.



Example – Board Design

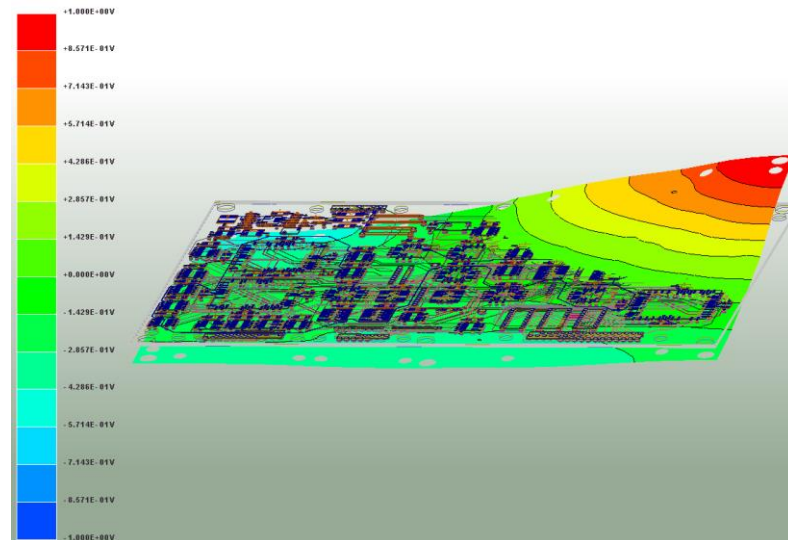
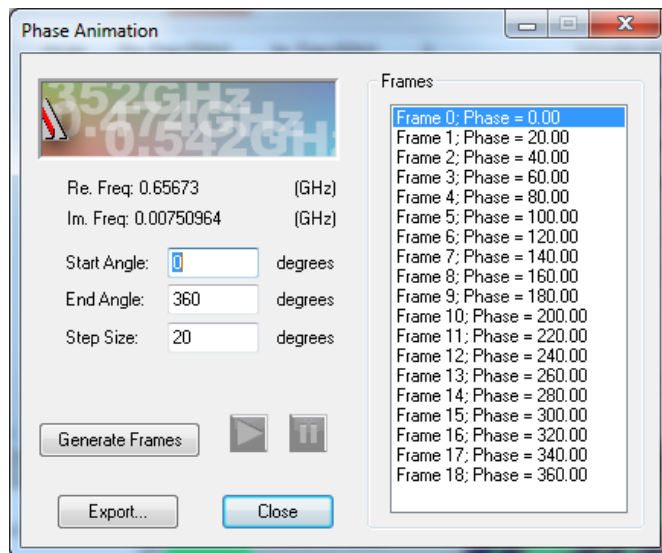
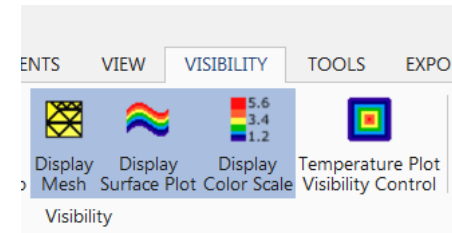
• Phase Animation

- In the Resonant Mode Results window, in the bottom section, highlight the **5th** resonant mode with Plot Layer **L2** and Reference Layer **L7**
- Click the **Phase Animation** button
 - Click the **Generate Frames** button
 - When all 20 frames are generated, Click the **Play** button
 - When done viewing the animation, click the **Close** button
- Click **Close** to close the Resonant Mode Results window

Note: To turn off the mesh display, click on the Display Mesh button

Note: To turn off the Display Color Scale click on the Display Color Scale button

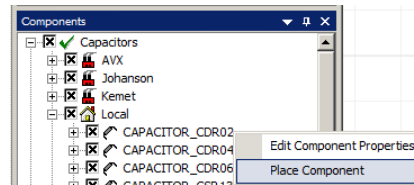
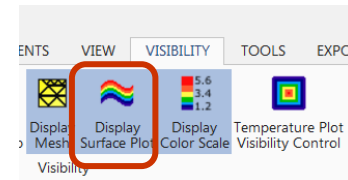
Note: The display can be rotated by holding down the **Alt** key and the **Left Mouse Button** and dragging.



Example – Board Design

• Adding Capacitors

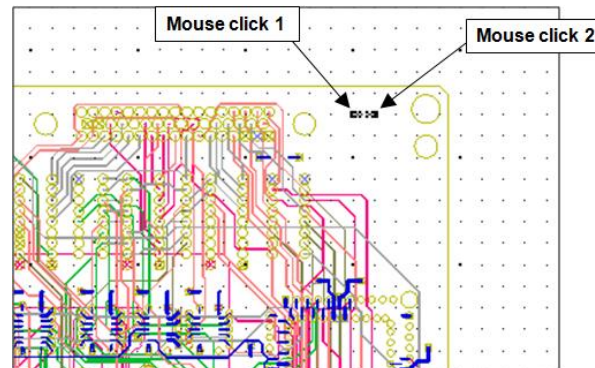
- At the 5th resonance, there is a large voltage swing that can be seen at the top right corner of the board. Capacitors will be added in that area to reduce the effect of the resonance.
- Click on the Home tab then select the Top-down View button
- To add capacitors:
 - Turn off the Surface Plot from the Visibility tab
 - Click with the right mouse button on the capacitor “CAPACITOR_CDR02” in the Components window as shown here



- The capacitor can be placed either graphically or for more precise positioning, the coordinates can be entered directly.



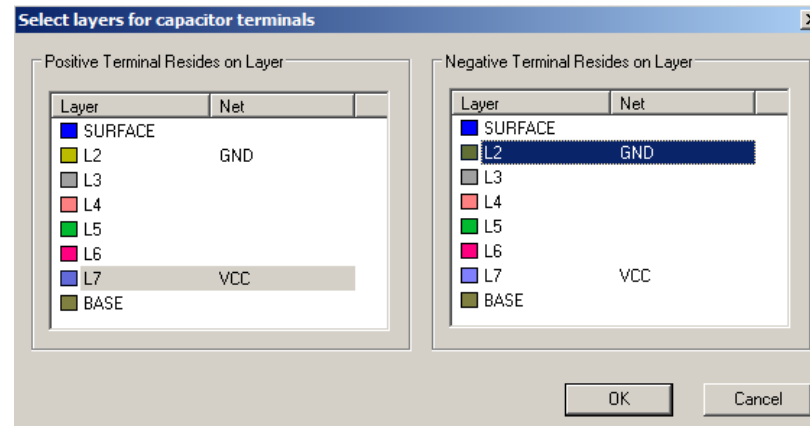
- For the current exercise it is sufficient to place the capacitor using the mouse as shown below. The exact location is not critical.



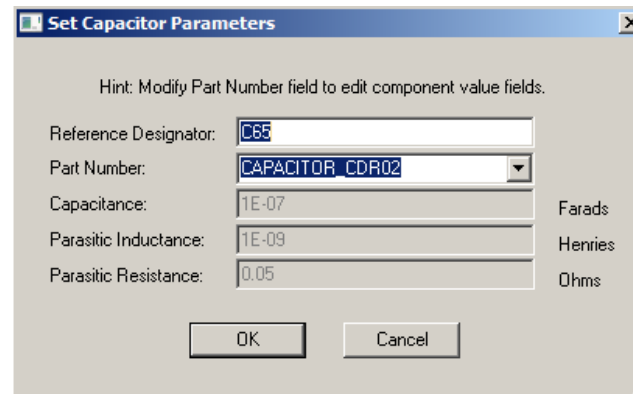
Example – Board Design

- **Adding Capacitors**

- When the capacitor has been placed, the following dialog window appears. This dialog defines the net connection and layer for the capacitor terminals.



- **Note:** that the capacitor can be directly connected to layers and nets inside the board. This is not possible in practice, but is useful to quickly see the effect of placing the components. The routing and/or via inductance could be added by introducing a new capacitor model with appropriate series inductance.
- For this exercise, the capacitors will not be modified. Click the **OK** button to accept the capacitor model.



Example – Board Design

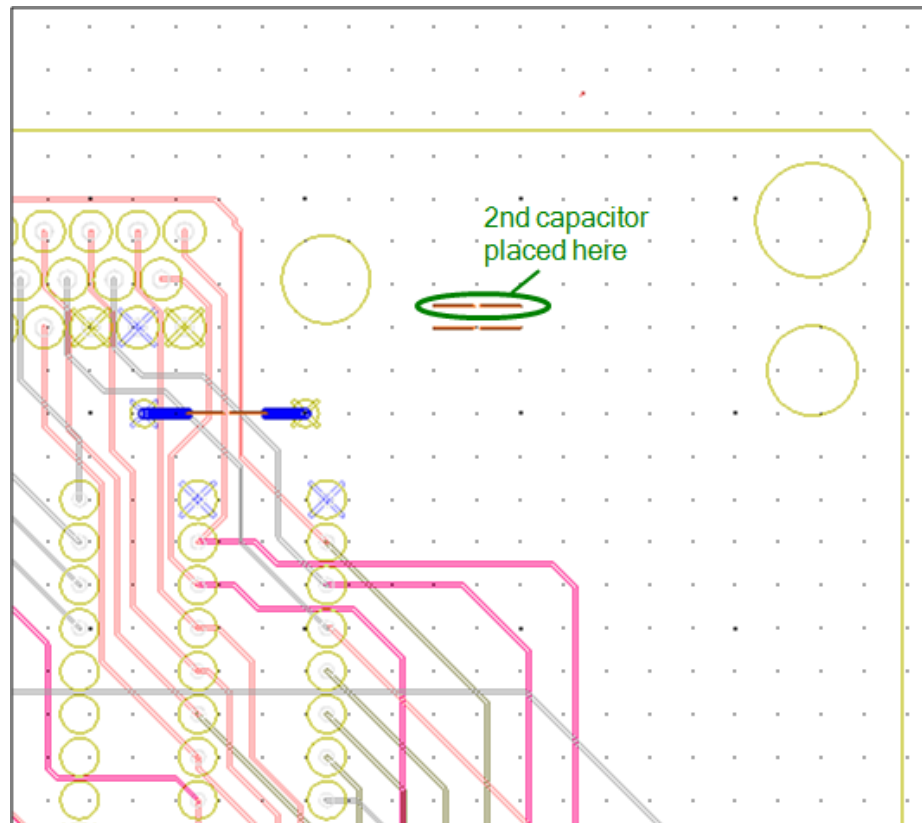
- **Adding Capacitors to the model**

- Place a 2nd capacitor, of the same type, just above the first one as shown here.
- The exact coordinates of the new capacitor terminals are:

x: 7800 y: 5250

x: 8000 y: 5250

- Again use the model **CAPACITOR_CDR02**.



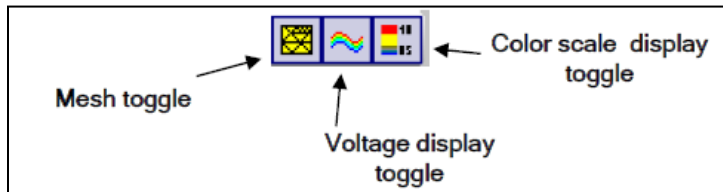
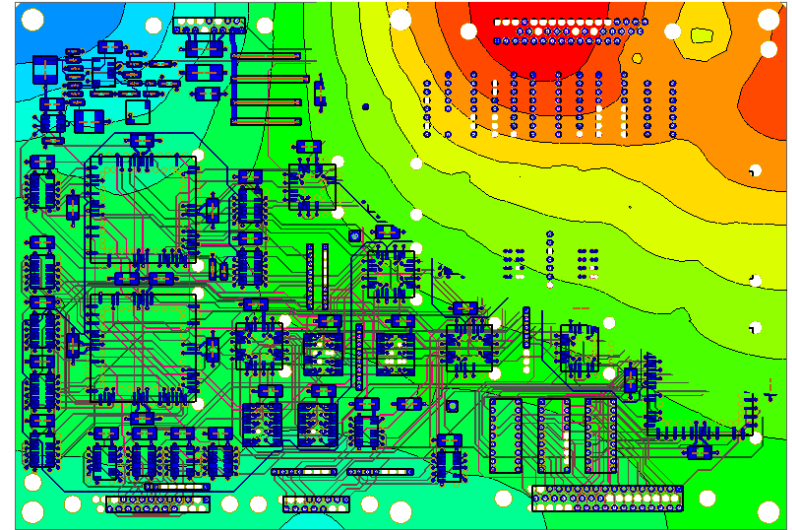
Example – Board Design

• Re-run the Resonant Mode Simulation

- Select the **Simulation Tab > Compute Resonant Modes**
 - Simulation Name: **Resonant Mode Sim 2**
 - Minimum Frequency: **2.55238E+008 (default)**
 - Maximum Frequency: **2E+009**
 - # of Modes to Compute: **5**
 - Click the **Launch** button

• Viewing Results

- Right-click on Resonant Mode Sim 2 and select **View Results**
 - Generate the voltage plot between planes **L2** and **L7** by selecting the layers as shown here and pressing **Compute**. This computation is required to generate the 2D plot from existing solution data.
 - View the 5th resonant mode plot again. The voltage amplitude at the top right corner of the board where the capacitors were placed shows reduced amplitude.
 - **Note:** The surface plot display may need to be turned on.



• Save the .siw file

- Select the menu item **File > Save**