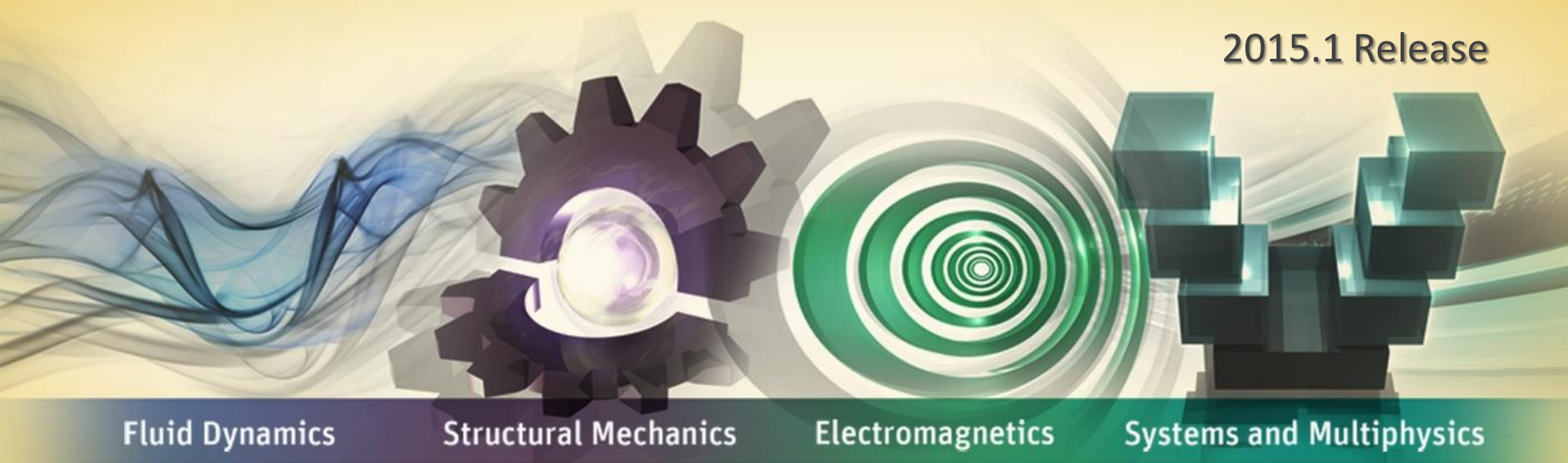


Workshop 7: SYZ for SI

2015.1 Release



Introduction to ANSYS SIwave

- **In this example you will learn and use the following skills:**

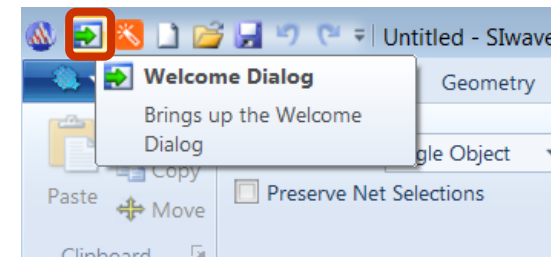
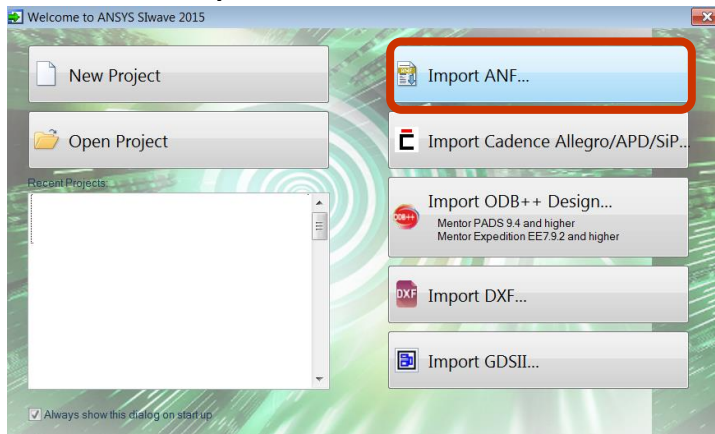
- Import an Ansoft Neutral Format (ANF) file and component file (CMP) and create an SIwave project
- Place ports on selected nets using an automated process
- Run an SYZ simulation and plot results for transmission, reflection, and crosstalk
- Export a Full-Wave SPICE sub-circuit
- Modify trace geometry to reduce crosstalk

- **Starting SIwave**

- To launch SIwave, click the Microsoft **Start** Button, select: **All Programs > ANSYS Electromagnetics > ANSYS Electromagnetics Suite 16.1 > ANSYS SIwave 2015.1**

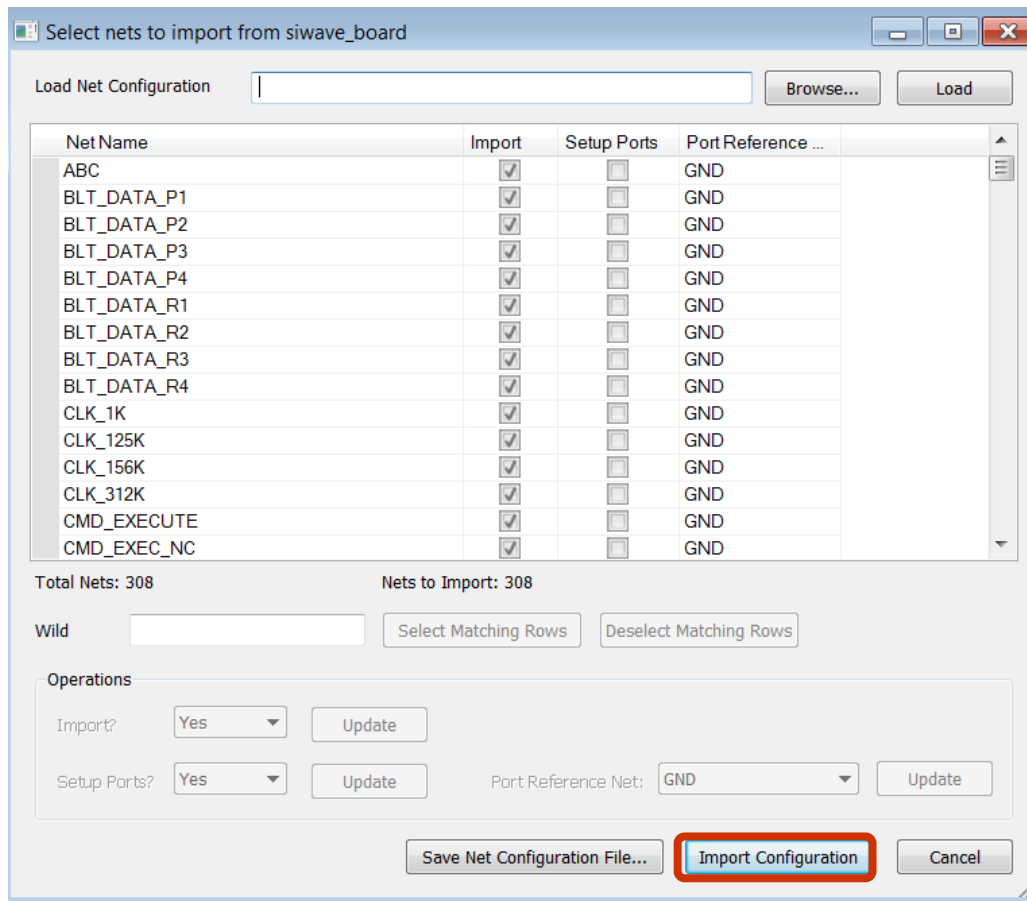
- **Import the .ANF (Ansoft Neutral File) file**

- Click the **Import ANF...** box
 - Navigate to the training files and choose : **siwave_board.anf**
 - Click the **Open** button

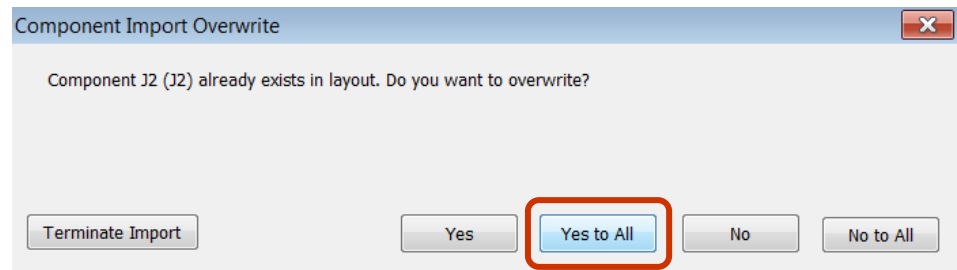
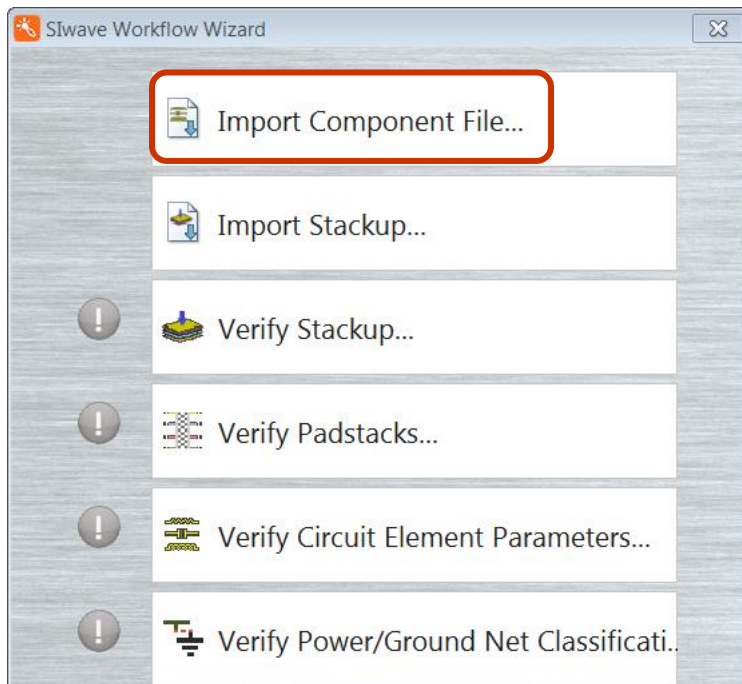


Siwave SYZ Analysis For SI

- The Select nets box will appear. (If desired, the user can filter nets to be imported. For this example, all nets will be imported)
 - Click the **Import Configuration** button



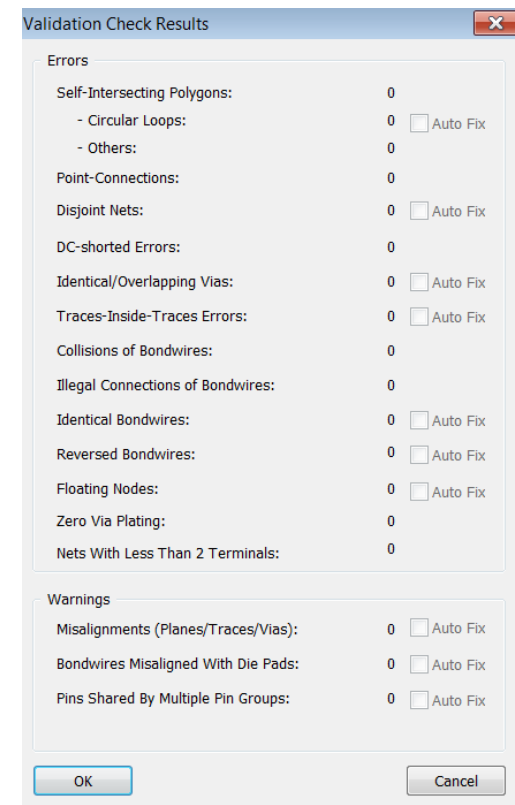
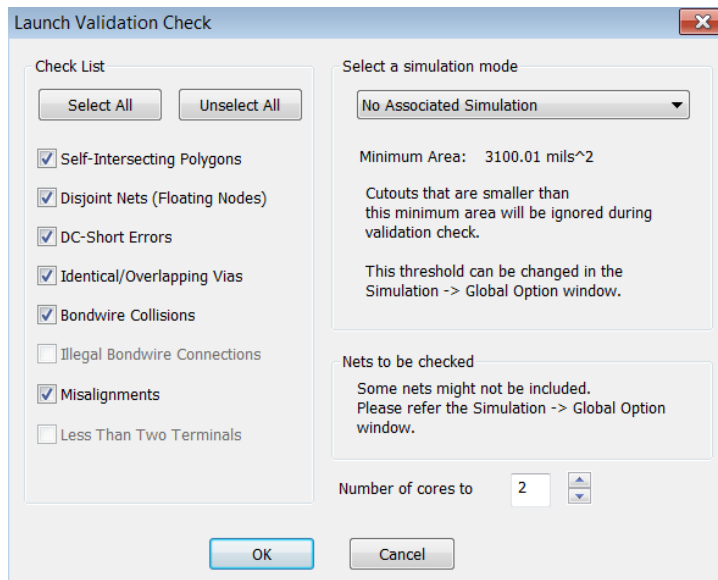
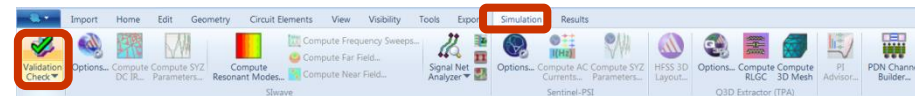
- The SIwave Workflow Wizard will appear
- Import the .cmp (Ansoft Component File)
 - Click on the **Import Component File...** button
 - Navigate to the training files and choose : **siwave_board.cmp**
 - Click the **Open** button
 - If there is a warning message click the **Yes to All** button to overwrite existing names
 - Close the Wizard and save the project



SYZ Parameters For Signal Integrity

• Validation Check

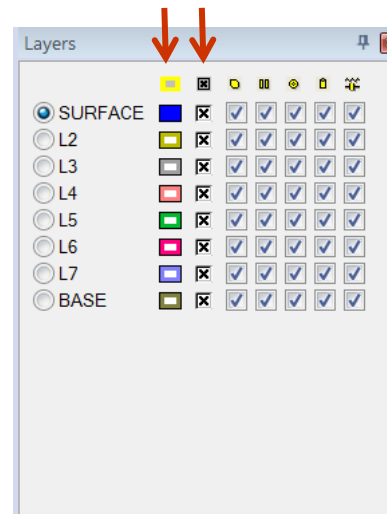
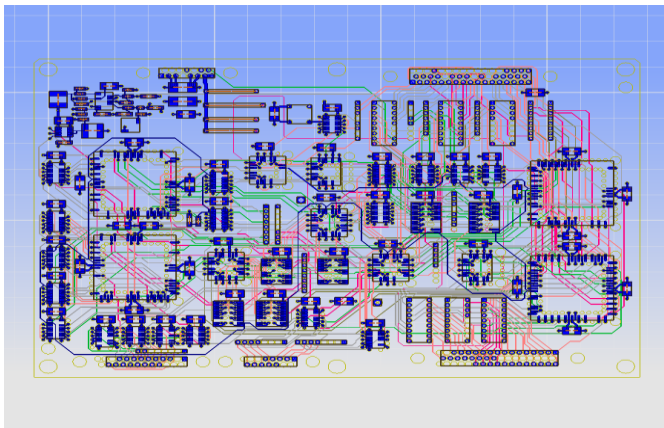
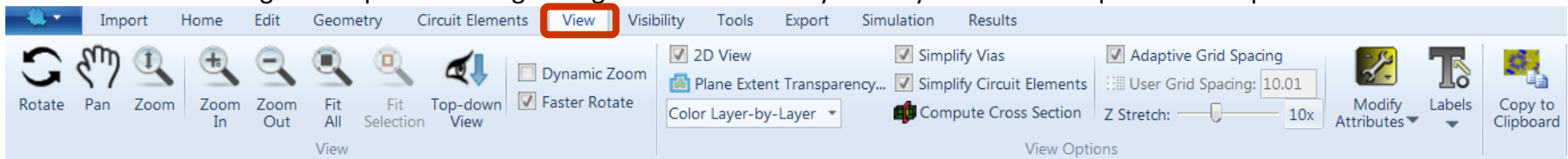
- It is a good idea to do a validation check before you start working on any design in SIwave for the first time
- The validation check tests for self-intersecting polygons, disjoint nets, overlapping (DC-shortened) nets and nets with overlapping vias.
- This helps you avoid finding layout errors after all the setting up ports and other solution settings.
- To do a validation check:
 - Go to the **Simulation** tab, select **Validation Check**.
 - Click **OK** button to start the validation
 - There are no layout and DRC related problem with this design.
 - Repeat this process if there are some **Misalignments** to verify that the **Auto Fix** worked
 - Click **OK**.



SYZ Parameters For Signal Integrity

• Set Visibility options

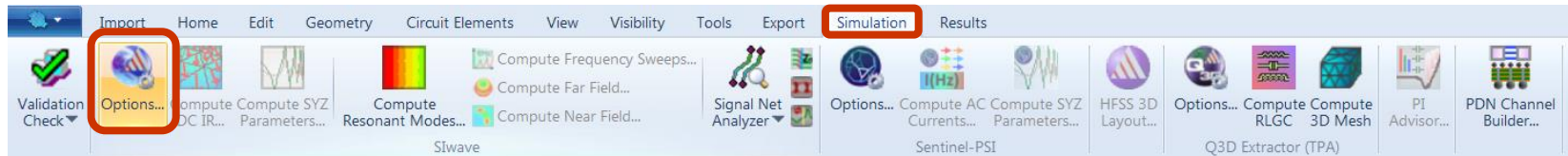
- Using the checkboxes in the **Layers** workspace, turn on full visibility of all layers
- Click the colored rectangles next to each layer name to control whether the geometry is shown in outline or filled form.
- Go to the **View** tab
 - Check **2D View** to view the project as a 2-dimensional entity
 - Check **Faster Rotate**
 - Uncheck **Dynamic Zoom**
 - Check **Simplify Circuit Elements**
 - Check **Simplify Vias**
- **Notes:** Selecting these options for large designs reduces memory used by SIwave and improve the response time.



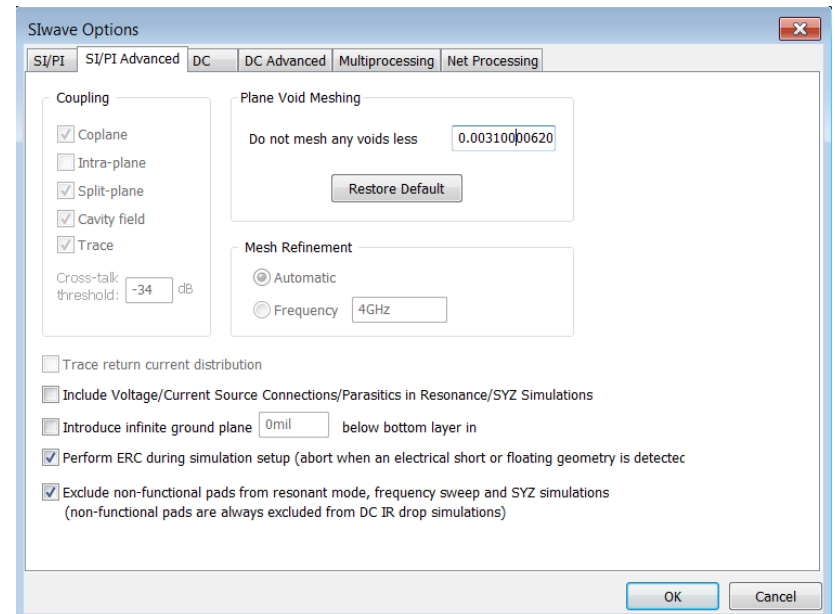
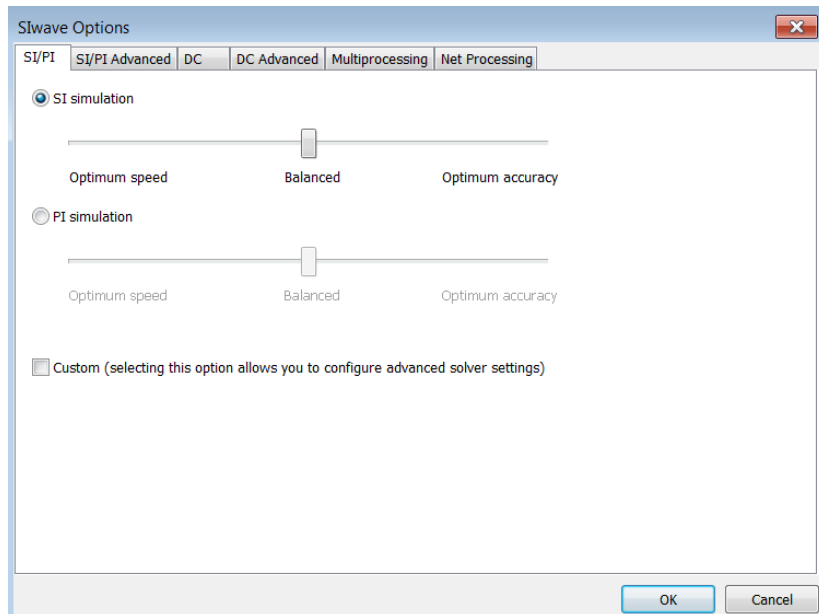
SYZ Parameters For Signal Integrity

• Setting Simulation Global Options

- From the **Simulation** tab, Select **Options**

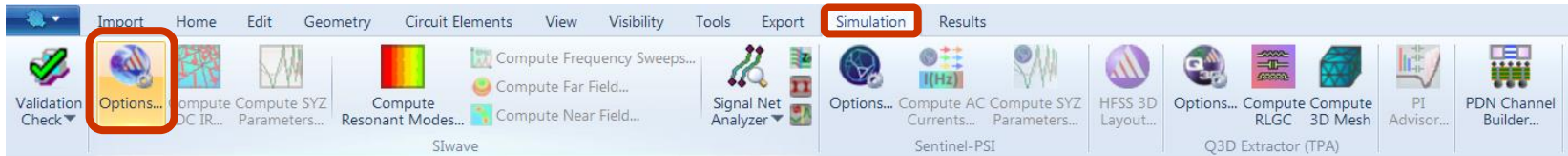


- Under **SI/PI** tab, let the slider bar of **SI simulation** to **Balanced**.
 - Note : To configure advanced solver settings Check **Custom**.
- Under **SI/PI Advanced** tab, look at the solver settings
 - Perform ERC during simulation setup: ☒ **Checked**
 - Exclude non functional pads : ☒ **Checked**

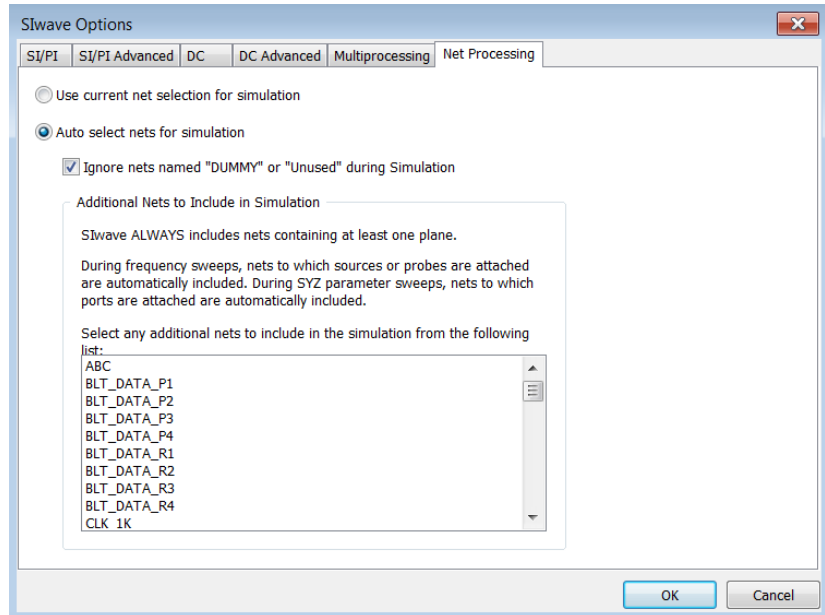
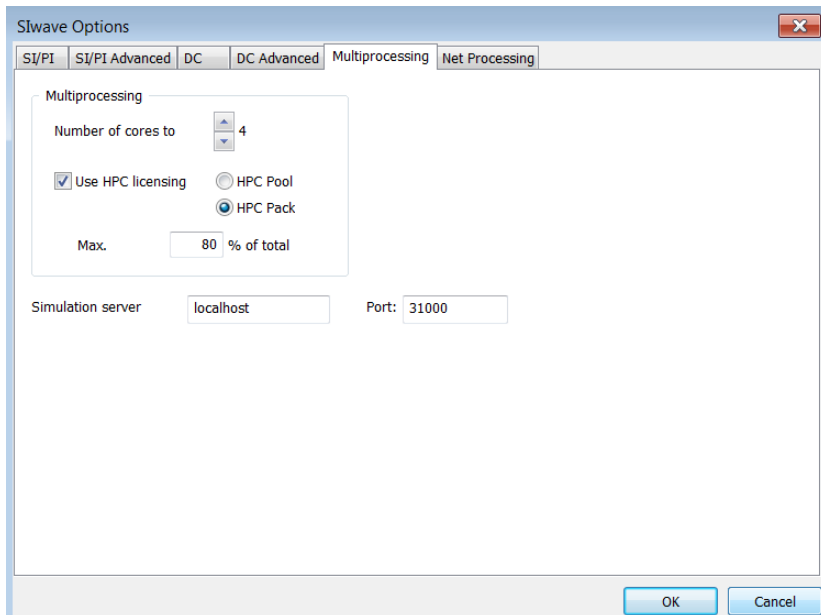


• Setting Simulation Global Options

- From the **Simulation** tab, Select **Options**



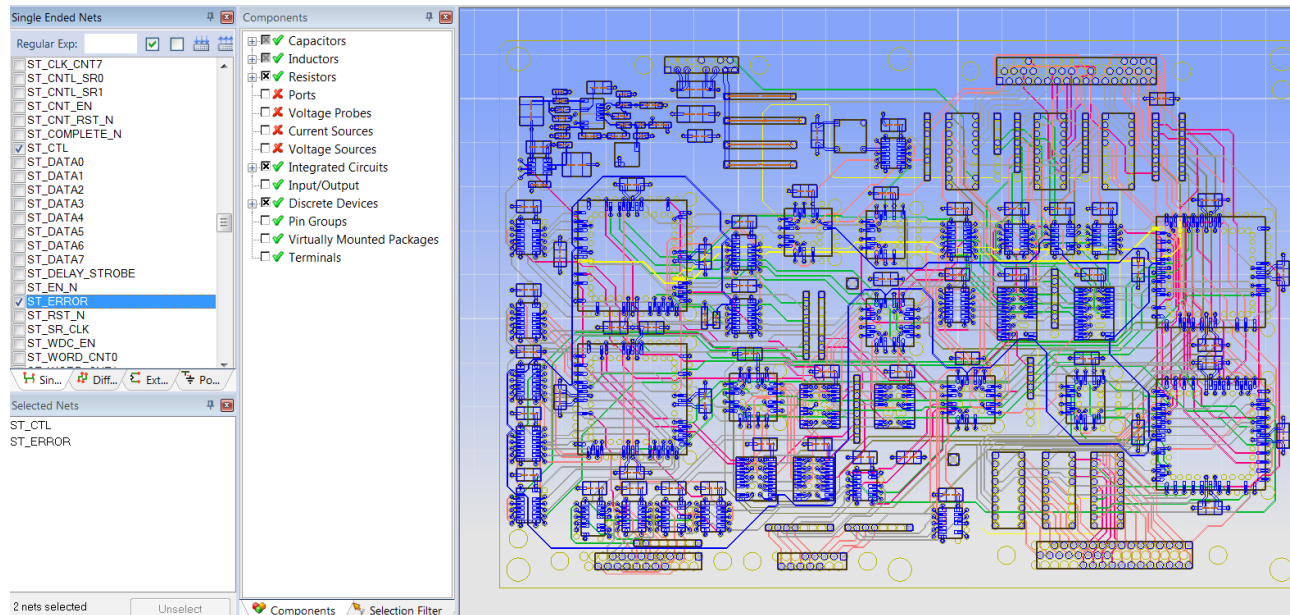
- Under **Multiprocessing** tab , set the number of cores you want to use
 - Check **Use HPC Licensing** to **HPC Pack** or **HPC Pool** if you have HPC licenses
- Under **Net Processing** tab
 - Ignore nets named “DUMMY” or “Unused” during Simulation: ☒ **Checked**
- Click **OK** button



SYZ Parameters For Signal Integrity

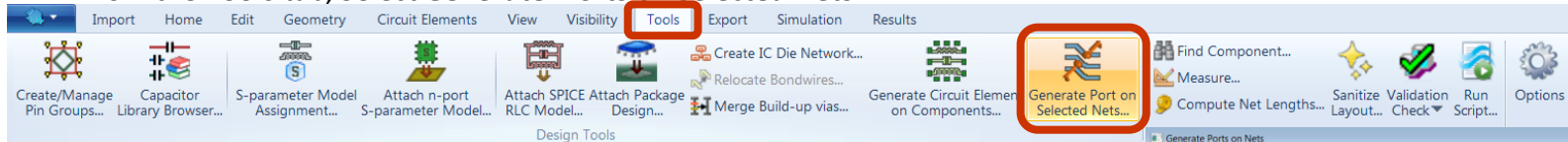
- **Add ports to the nets of interest**

- Ports are elements that enable the entry and exit of electromagnetic energy in a design. We will add ports at both ends of two coupled traces.
- In the **Single Ended Nets** workspace, scroll down until you find the **ST_CTL** and **ST_ERROR** nets
- Place check marks next to
 - **ST_CTL**
 - **ST_ERROR**
- The nets will show up in the **Selected Nets** workspace.
- The nets should now be highlighted. For the most part, they run horizontally on layer L3
 - You can also highlight nets by checking the checkbox next to Nets in the **Selection Filter** workspace and then clicking on the nets in the layout window

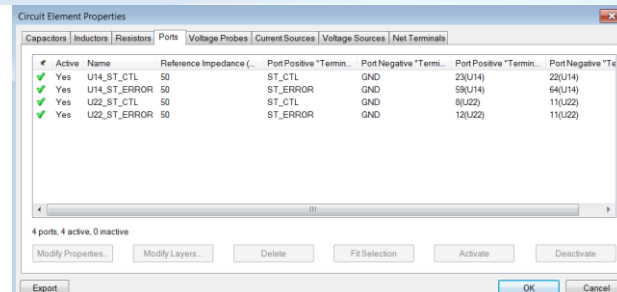
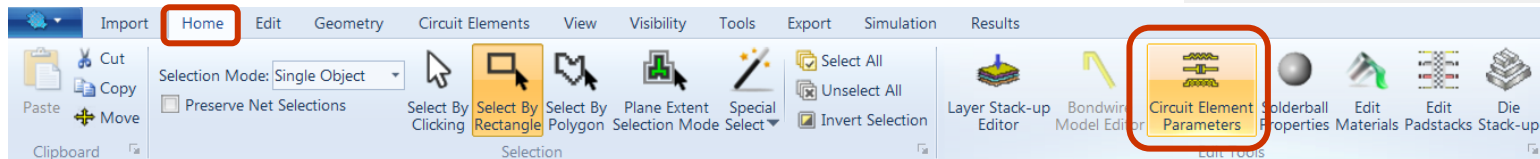
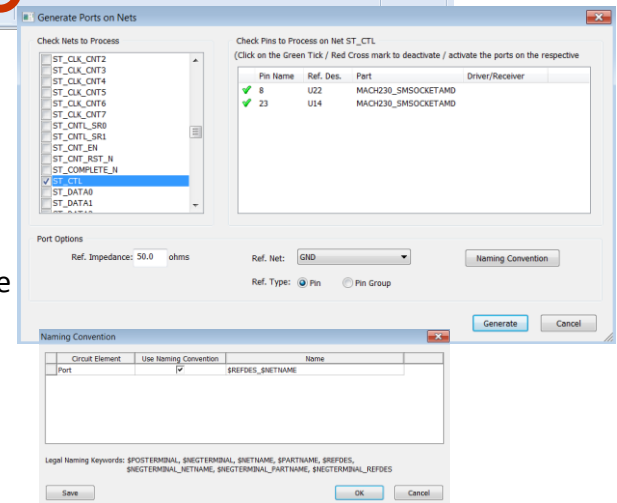


• Generate Ports

- From the **Tools** tab, Select **Generate Ports on Selected Nets...**



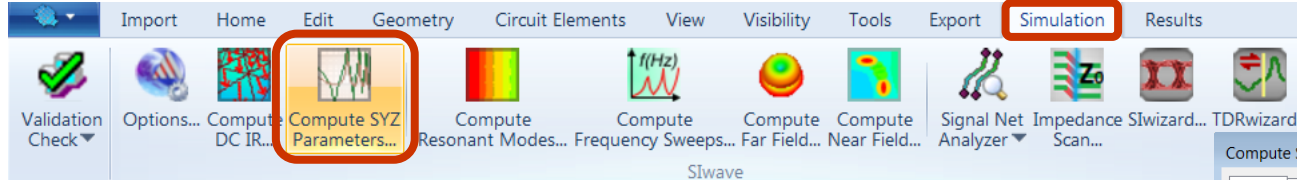
- Click the **Naming Convention** button:
 - Enter Port naming convention: **\$REFDES_\$NETNAME**
 - Select **Use Naming Convention** ☒
 - Press the **OK** button
- Make sure the **Ref. Net** is set to **GND**
- Click the **Generate** button to automatically create 50 ohm ports at each end of the
- Verify that the 4 ports have been properly created
 - From the **Home** tab, Select **Circuit Element Parameters...**
 - Select the **Ports** tab
 - Click **OK**



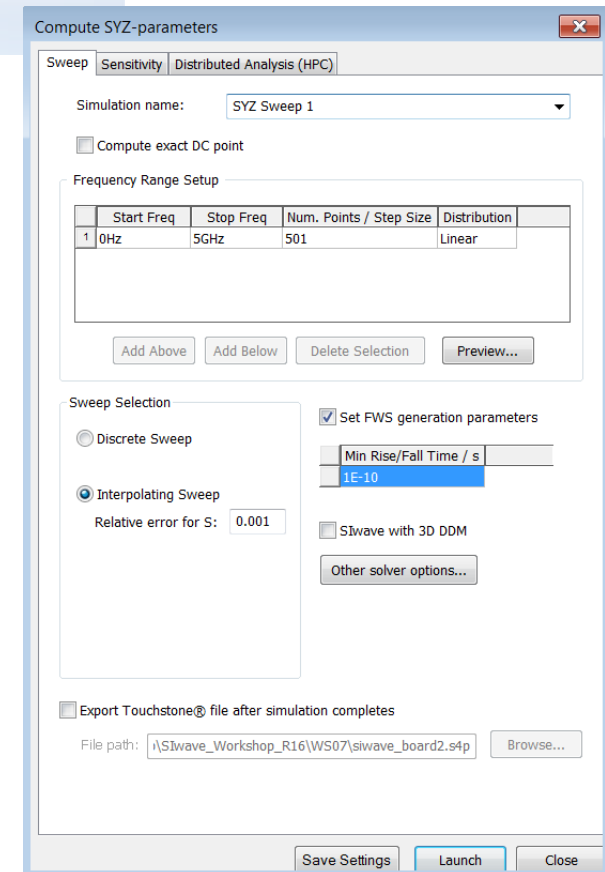
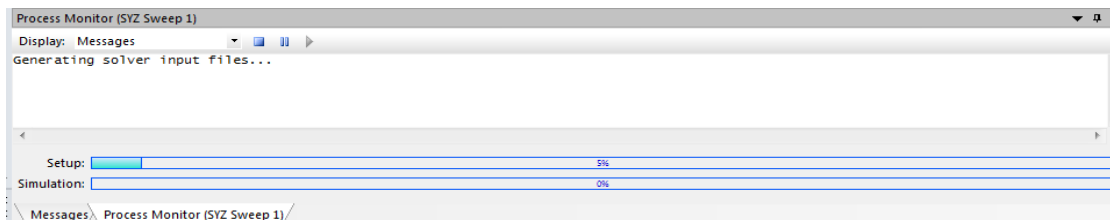
SYZ Parameters For Signal Integrity

• Run an SYZ Simulation

- Form the menu **Simulation**, select **Compute S-, Y-, Z-Parameters...**



- Change the settings as shown below:
 - Start Freq: **0 Hz** and Stop Freq: **5GHz**
 - Num. Points: **501** and Distribution: **Linear**
 - Sweep Selection:
 - Option button: **Interpolating Sweep**
 - Error Tolerance: **0.001**
 - Set FWS generation parameters: ☒ **Checked**
 - Uncheck **Export Touchstone file after simulation completes**
- Click the **Launch** button to start the simulation
- Wait for the simulation to complete



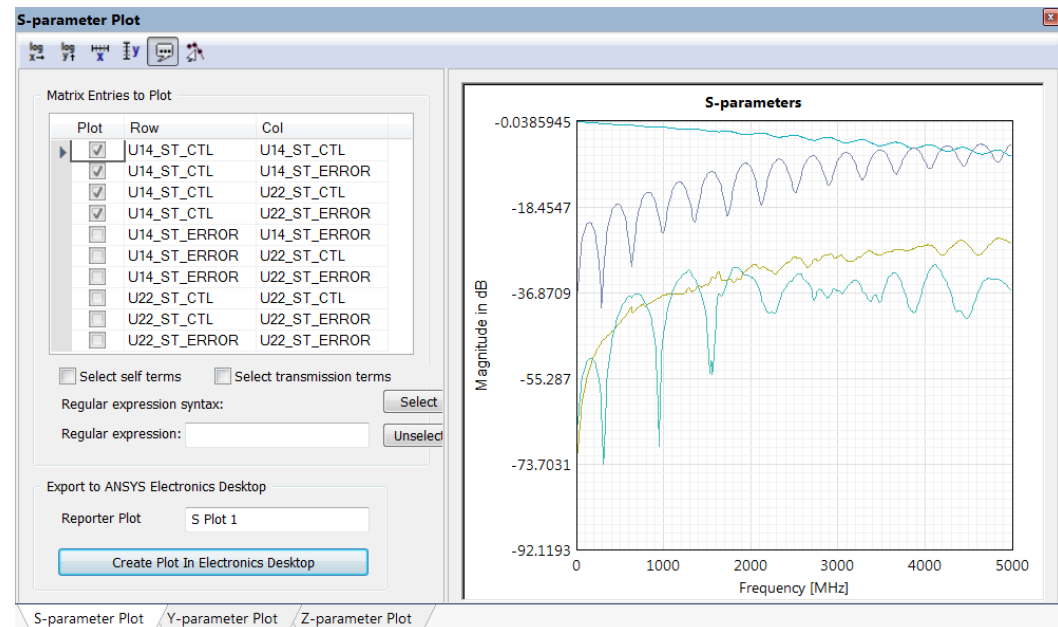
SYZ Parameters For Signal Integrity

Plot the results

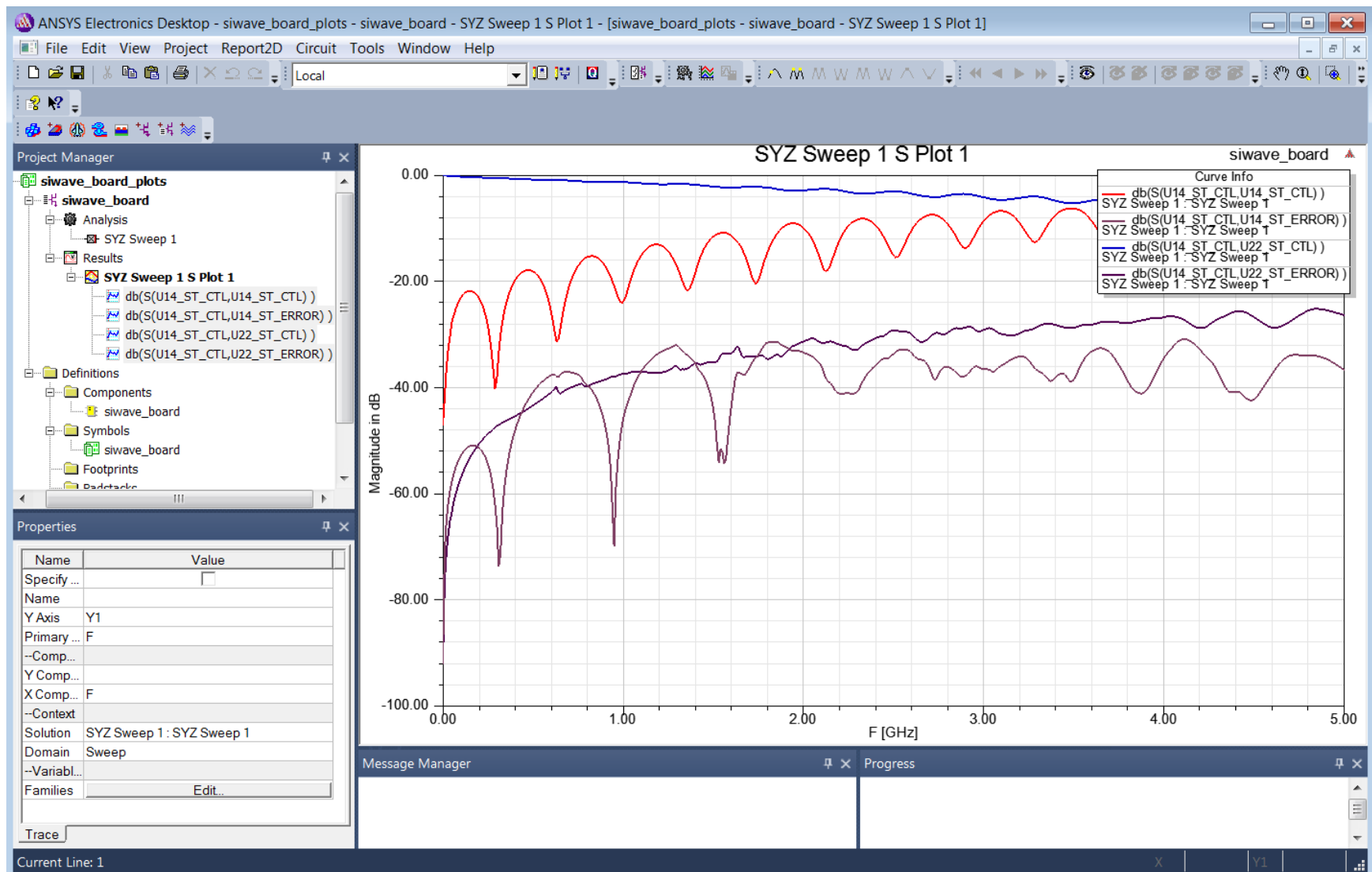
- When the simulation has finished, plot the results
- From the **Results** tab, Select **SYZ > SYZ Sweep 1 > Plot Magnitude/Phase...**



- Uncheck the **Select Transmission Terms** checkbox to clear the plot
- Uncheck the **log x->** button in the top left corner
- Check the following four boxes in the list:
 - **U14_ST_CTL, U14_ST_CTL**
 - **U14_ST_CTL, U22_ST_CTL**
 - **U14_ST_CTL, U14_ST_ERROR**
 - **U14_ST_CTL, U22_ST_ERROR**
- Click the **Create Plot in Electronics Desktop** button



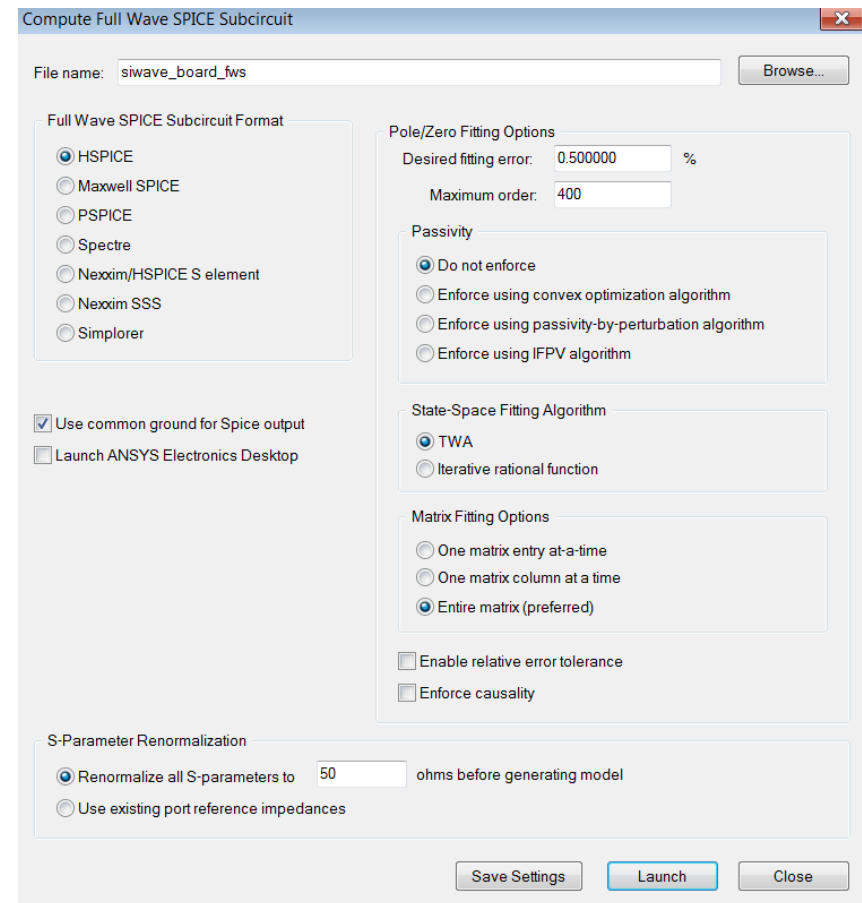
SYZ Parameters For Signal Integrity



SYZ Parameters For Signal Integrity

- **Export a Full-Wave SPICE sub-circuit model**

- Close the **ANSYS Electronics Desktop**
- Close the **Results** Viewer
- From the **Results** tab , Select **SYZ > SYZ Sweep 1 > Compute FWS sub-circuit**
 - File name: **siwave_board_fws**
 - Full Wave Spice Subcircuit Format: **HSPICE**
 - Use common ground for Spice output: ☒ **Checked**
 - Click the **OK** button



Compute Full Wave SPICE Subcircuit

File name:

Full Wave SPICE Subcircuit Format

☒ HSPICE
☐ Maxwell SPICE
☐ PSPICE
☐ Spectre
☐ Nexxim/HSPICE S element
☐ Nexxim SSS
☐ Simplorer

☒ Use common ground for Spice output
☐ Launch ANSYS Electronics Desktop

Pole/Zero Fitting Options

Desired fitting error: %
Maximum order:

Passivity

☒ Do not enforce
☐ Enforce using convex optimization algorithm
☐ Enforce using passivity-by-perturbation algorithm
☐ Enforce using IFPV algorithm

State-Space Fitting Algorithm

☒ TWA
☐ Iterative rational function

Matrix Fitting Options

☐ One matrix entry at-a-time
☐ One matrix column at a time
☒ Entire matrix (preferred)

☐ Enable relative error tolerance
☐ Enforce causality

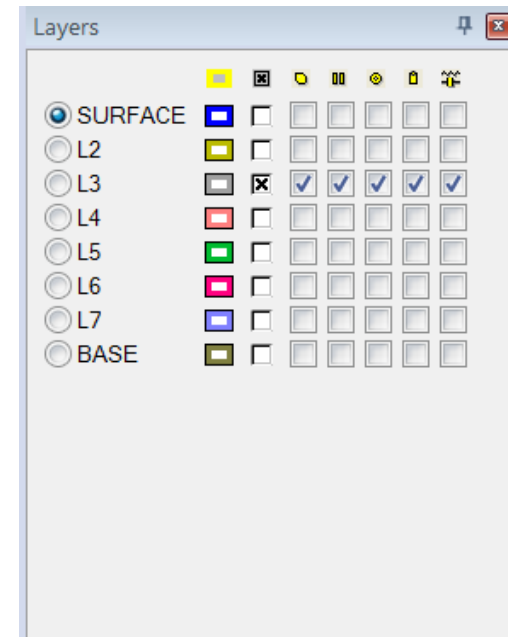
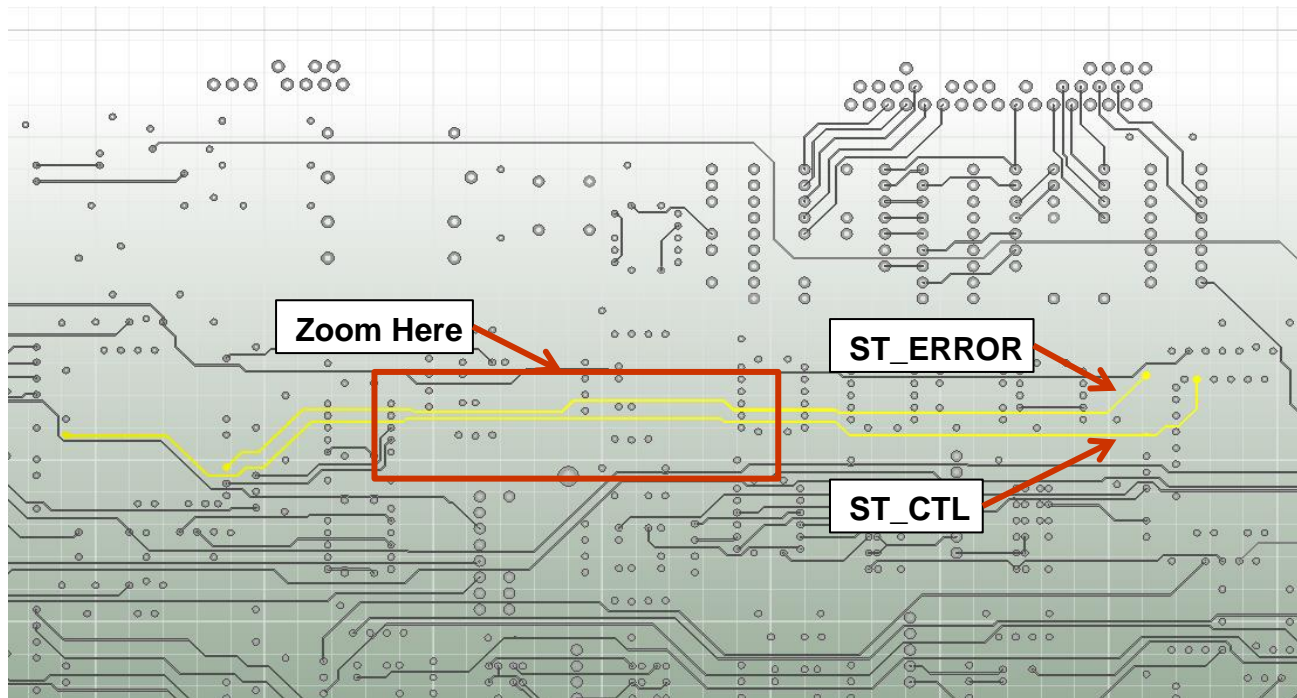
S-Parameter Renormalization

☒ Renormalize all S-parameters to ohms before generating model
☐ Use existing port reference impedances

SYZ Parameters For Signal Integrity

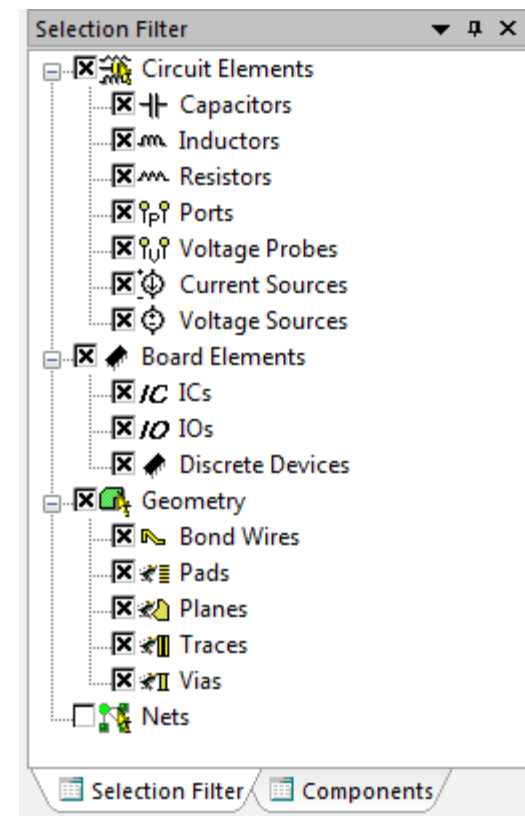
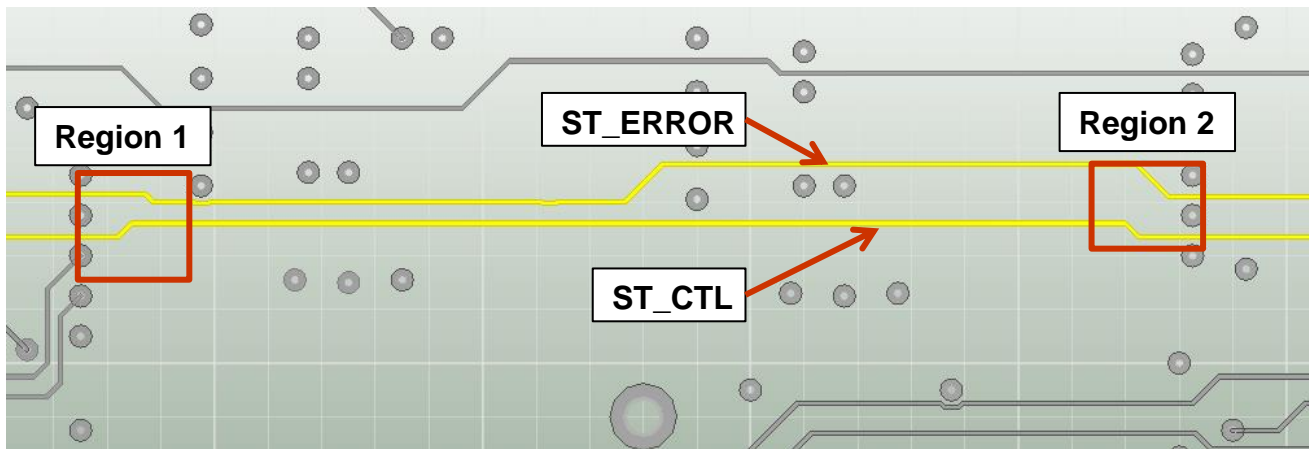
- **Edit the traces to lower crosstalk**

- The S-parameter results show fairly low near-end crosstalk, but we'll assume that a system simulation using the model indicated a need to reduce the coupling. We will edit the traces by increasing the minimum spacing between them to attempt to lower the crosstalk.
- Use the checkboxes in the Layers workspace to turn off the visibility of all layers except for L3 on which the ST_CTL and ST_ERROR traces are routed.
 - If the ST_CTL and ST_ERROR nets are not still highlighted, highlight them by clicking the boxes next to their names in the Nets workspace. The main window should look roughly like that below.
 - Zoom into the region outlined in the black box below.



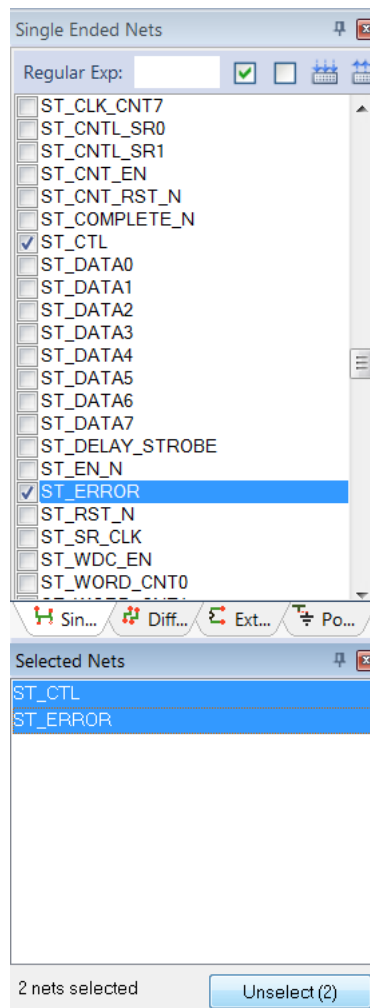
SYZ Parameters For Signal Integrity

- Now the main window shows a portion of the ST_CTL and ST_ERROR nets where they are routed close together.
- In the **Selection Filter** workspace, ensure that the box next to Geometry is checked.
- Zoom into the area labeled Region 1 in the above figure. The top left corner of Region 1 is at approximately (2700, 3340) mils.



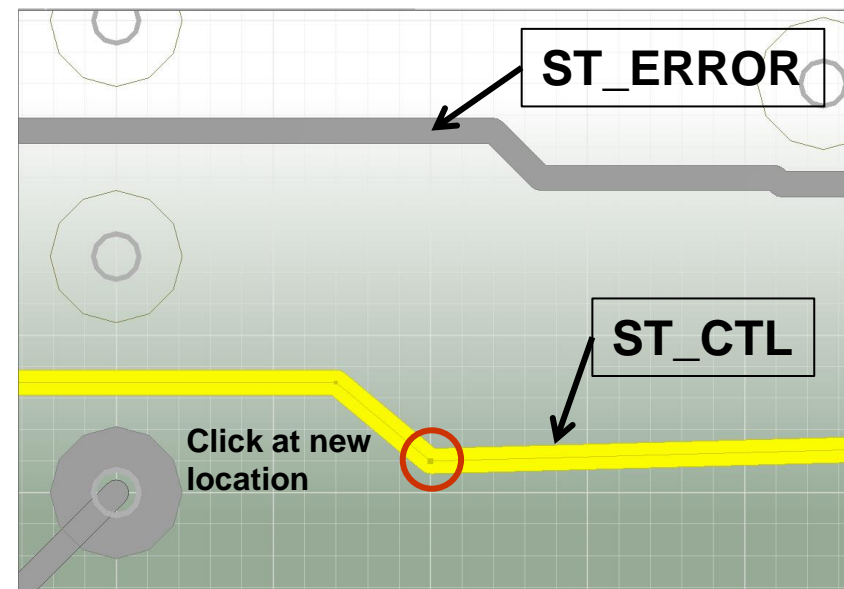
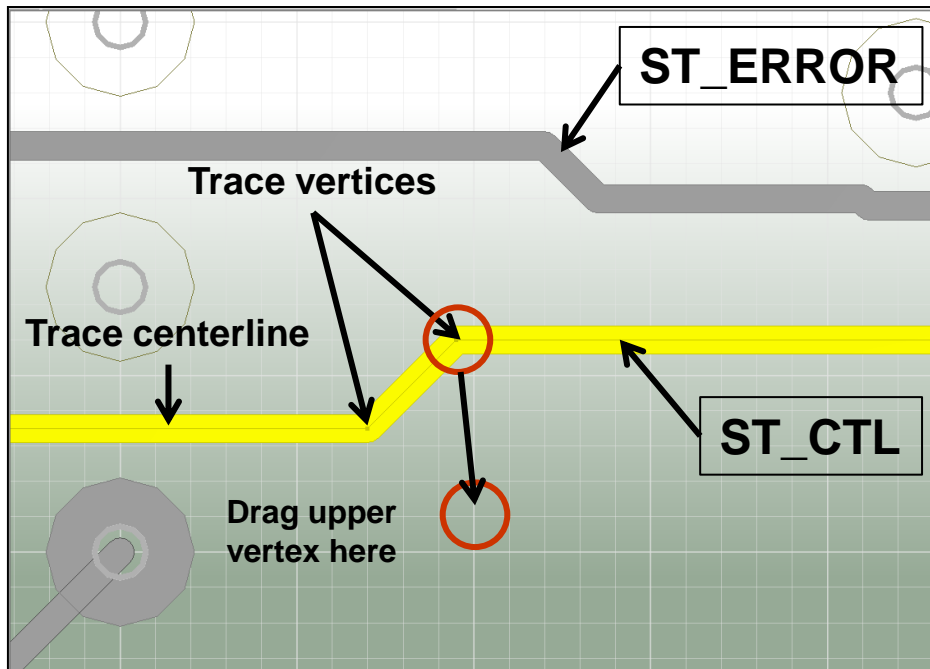
SYZ Parameters For Signal Integrity

- Unselect the selected nets by selecting both of the nets in the **Selected Nets** sidebar box and press the **Unselect** button. This will allow the nets to be manipulated.



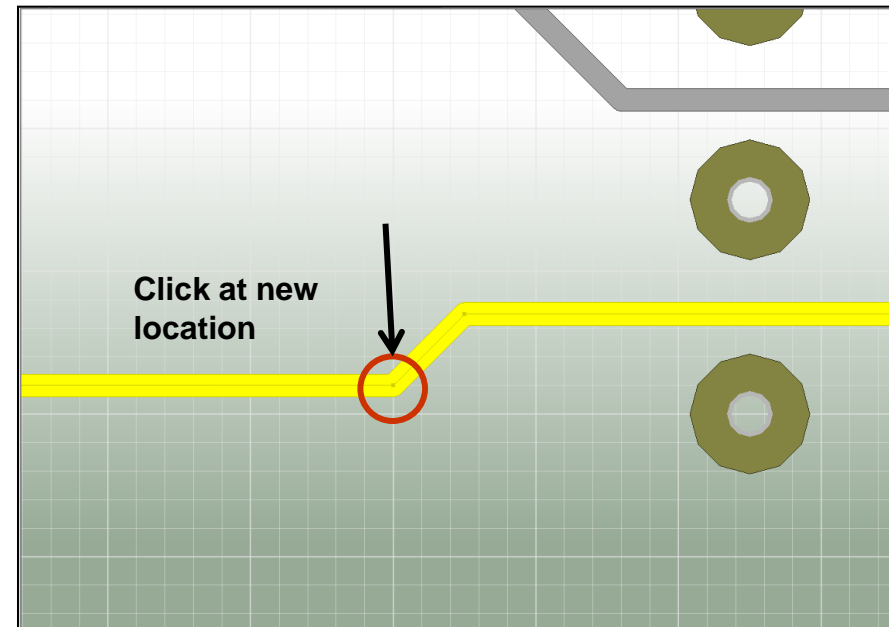
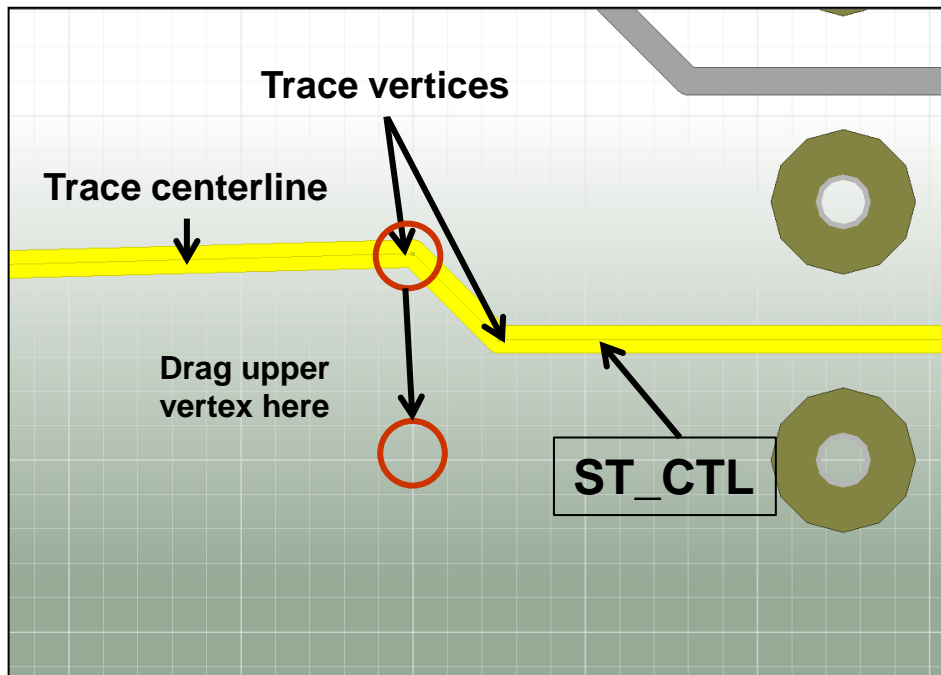
SYZ Parameters For Signal Integrity

- Click on the ST_CTL trace. The ST_ERROR net will de-highlight.
- Click again on the ST_CTL trace and the trace vertices and centerline will become visible.
- Drag the upper vertex within Region 1 to the location shown, approximately coordinates (2850, 3210) mils.
- Click on the new location to place the vertex.



SYZ Parameters For Signal Integrity

- Zoom out, then zoom into Region 2, which has an upper left corner at approximate coordinates (4660, 3300) mils.
- Click on net ST_CTL to highlight the trace.
- Click on the trace again to display the trace vertices and centerline.
- Drag the upper vertex to the location shown in the figures, approximately (4700, 3210) mils.
- Click on the location to place the vertex.



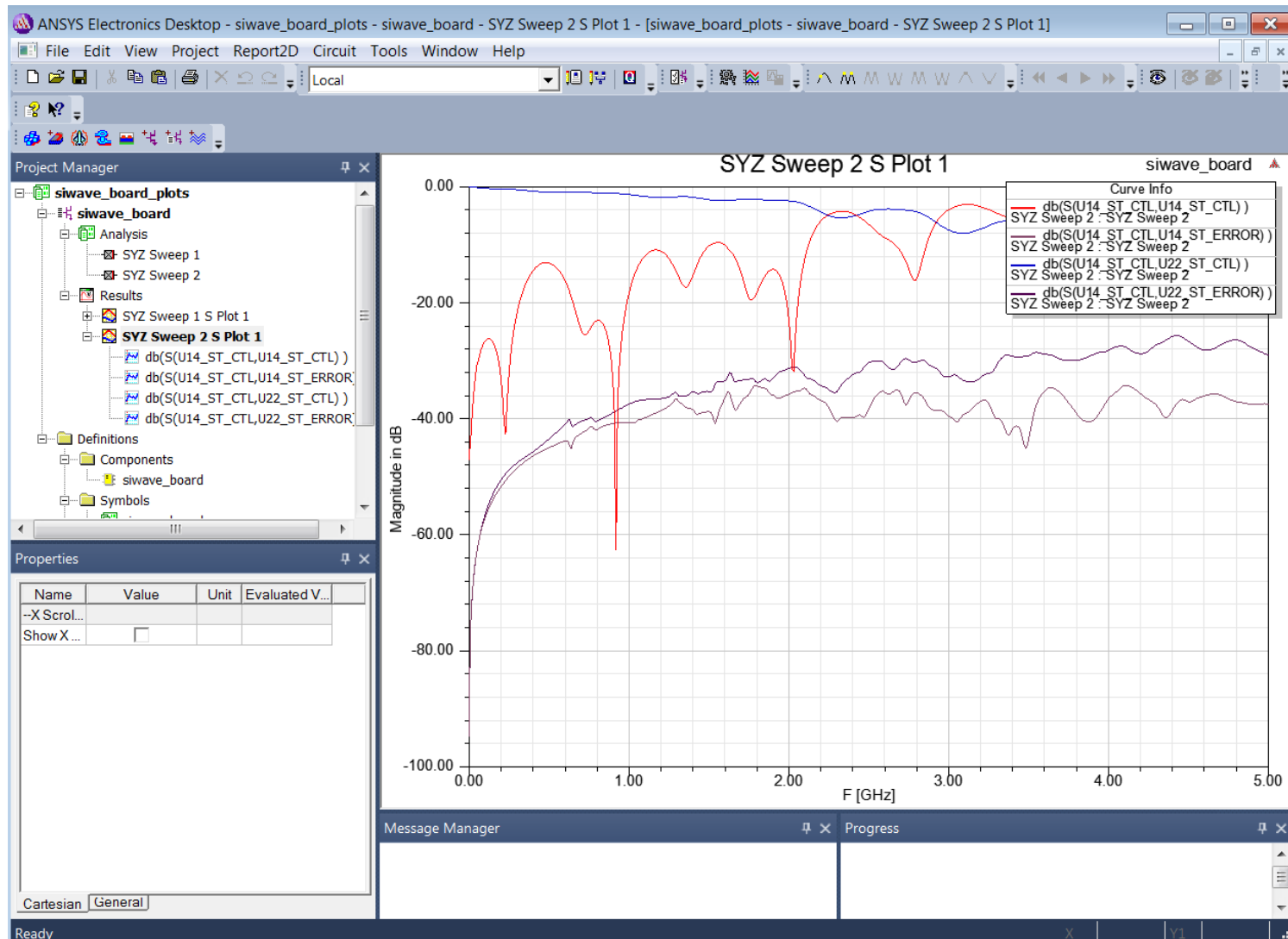
- **Re-run the simulation**

- From the menu *Simulation*, select *Compute S-, Y-, Z-Parameters...*
 - Enter **SYZ Sweep 2** in the Simulation Name field.
 - Uncheck *Export Touchstone file after simulation completes*
 - Keep the other settings the same as the first simulation
 - Click **Launch**

- **Plot the new results**

- From the *Results* tab, Select *SYZ > SYZ Sweep 2 > Plot Magnitude/Phase...*
 - Repeat the earlier process for selecting the four matrix entries in the list and click the **Create Plot in Electronics Desktop** button
 - The trace modification has slightly reduced the peak crosstalk. The frequency at which crosstalk first exceeds -32dB is roughly 1.2GHz in the original design, and 2GHz in the modified design.
 - Save the modified design
 - Click *File > Save As...*
 - Filename: **siwave_board2.siw**
 - Click **Save**

SYZ Parameters For Signal Integrity



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