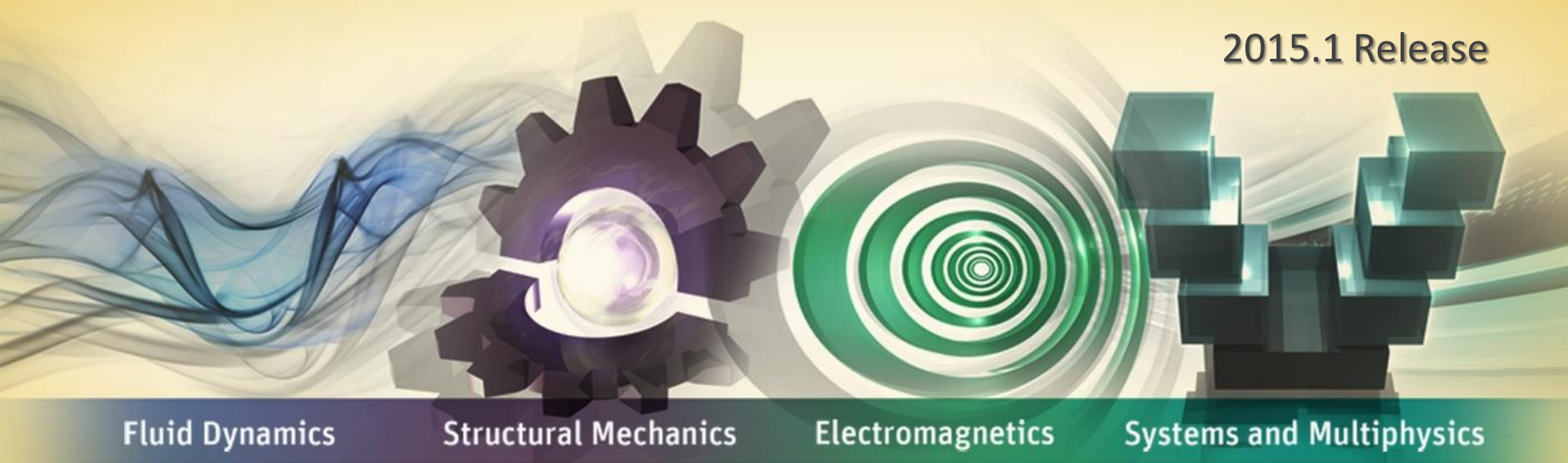


Workshop 3: Package SYZ Analysis

2015.1 Release



Introduction to ANSYS SIwave

- **Package S-parameters**

- The example is intended to show you how to simulate S-parameters on a 4 layer package structure using SIwave.
- You will learn how to:
 - Create ports using automatic port generation feature
 - Compute S-parameters
 - Simulate crosstalk with Touchstone file in ANSYS Electronics Desktop
 - Compute differential S-parameters
 - Export Full Wave Spice (frequency dependent) subcircuit
 - Export RLGC subcircuit

- **ANSYS SIwave Design Environment**

- The following features of the ANSYS SIwave Design Environment are used to create this passive device model
 - Pre-processing
 - Automatic ports generation
 - Boundaries/Sources
 - Ports
 - Solutions
 - S-Parameters
 - Differential S-parameter
 - Crosstalk (transient) simulation with ANSYS Designer
 - Plots
 - S-Parameter sweep
 - Differential S-Parameter sweep
 - Export
 - Full Wave Spice subcircuit
 - RLGC matrices and subcircuit

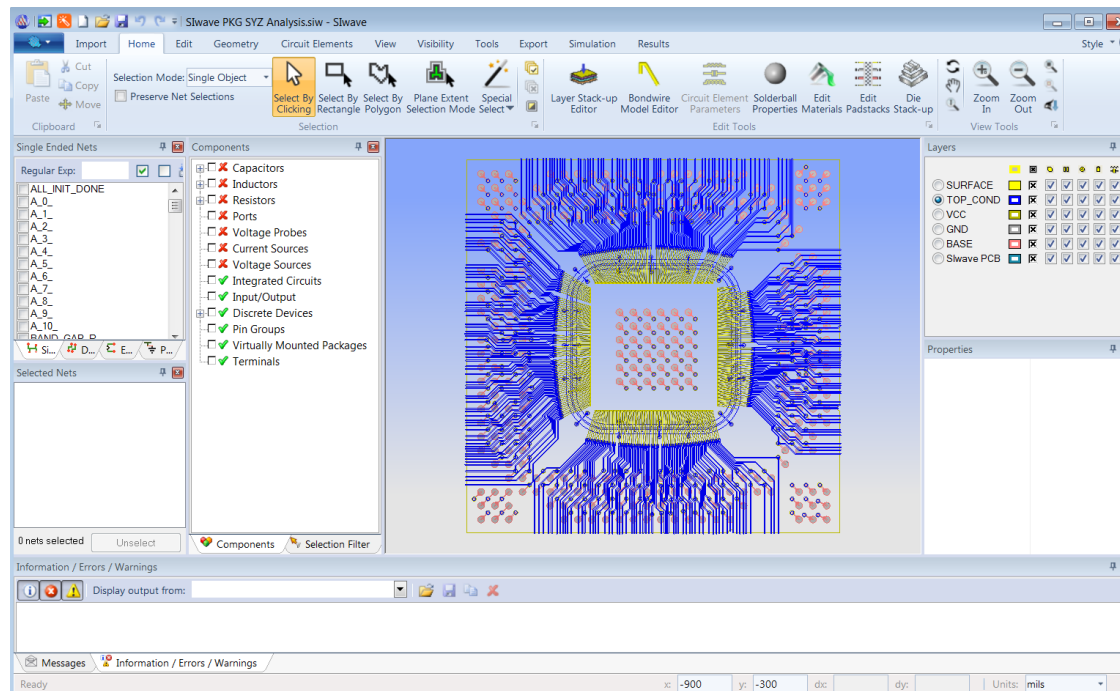
Package S-parameters

• Starting SIwave

- To launch SIwave program, click the **Start** button and select **All Programs > ANSYS Electromagnetics > ANSYS Electromagnetics Suite 16.1 > ANSYS SIwave 2015.1**

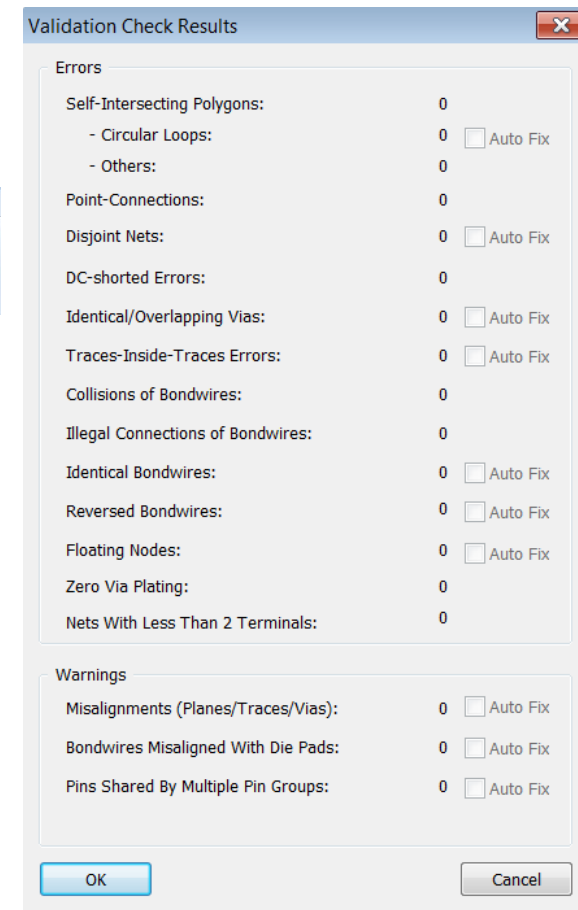
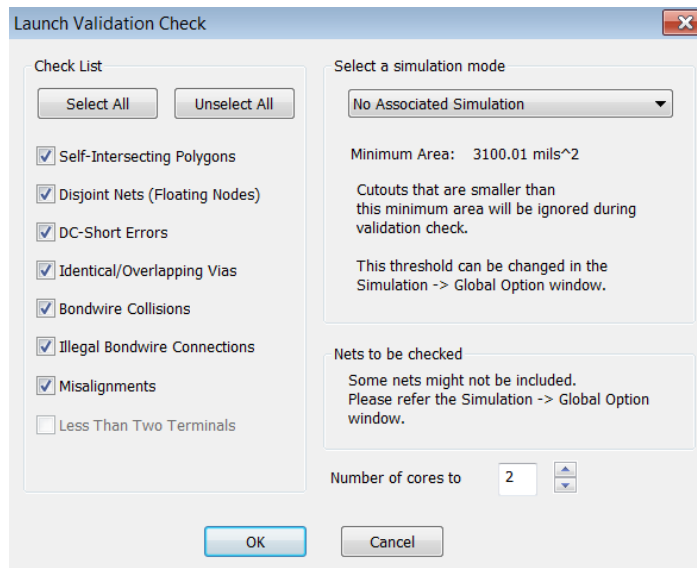
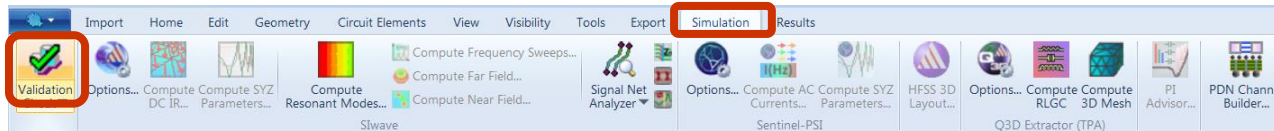
• Open a SIwave Project

- Click the **Open Project** box
 - Navigate to the training files and choose : **SIwave PKG SYZ Analysis.siw**
- This project has the correct dimensions and materials for layer stack up, bond wires, and solder balls.



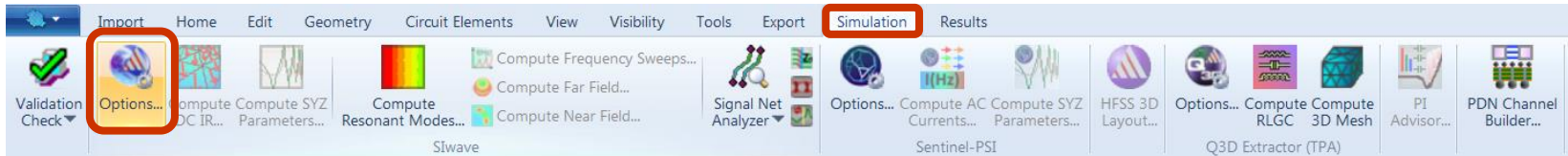
• Validation Check

- It is a good idea to do a validation check before you start working on any design in SIwave for the first time
- The validation check tests for self-intersecting polygons, disjoint nets, overlapping (DC-shortened) nets and nets with overlapping vias.
- This helps you avoid finding layout errors after all the setting up ports and other solution settings.
- To run the validation, go to the **Simulation** tab, select **Validation Check**.
 - Click the **OK**
 - There are no layout and DRC related problem with this design.
 - Click the **OK** button to exit the Validation Check Results dialog.

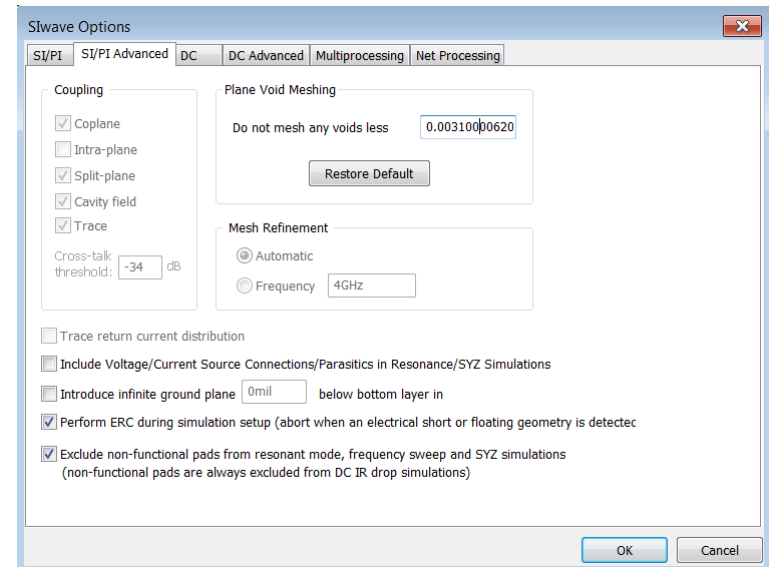
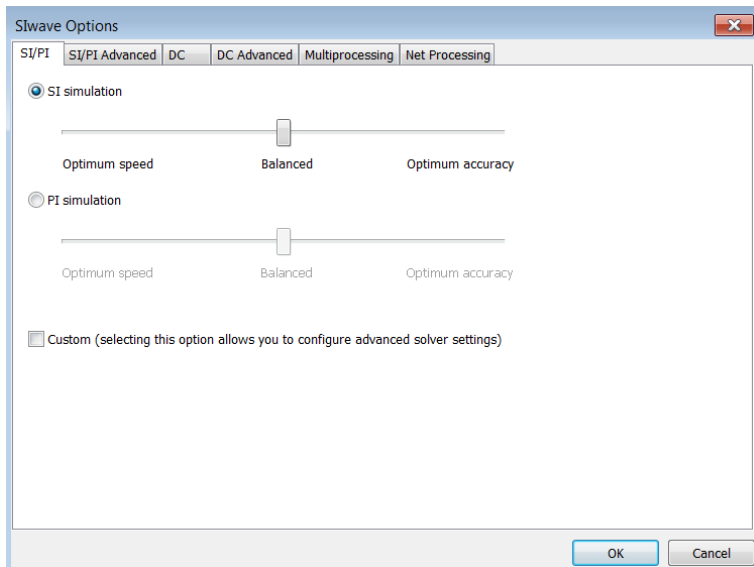


• Setting Simulation Global Options

- From the **Simulation** tab, Select **Options**

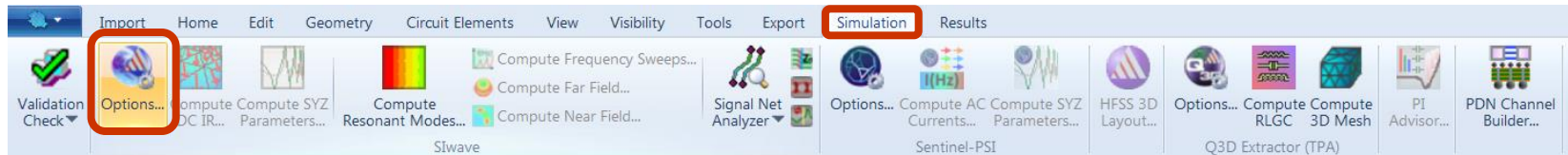


- Under **SI/PI** tab, let the slider bar of **SI simulation** to **Balanced**.
 - Note : To configure advanced solver settings Check **Custom**.
- Under **SI/PI Advanced** tab, look at the solver settings
 - Perform ERC during simulation setup: ☒ **Checked**
 - Exclude non functional pads : ☒ **Checked**

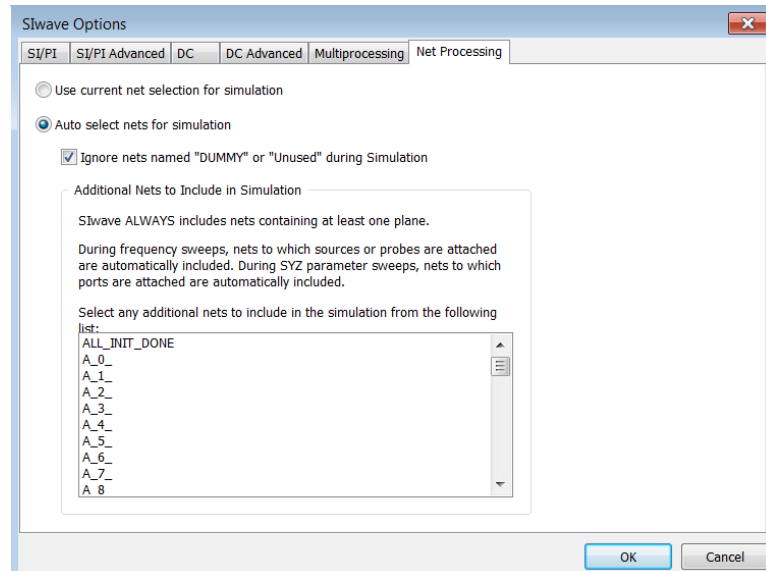
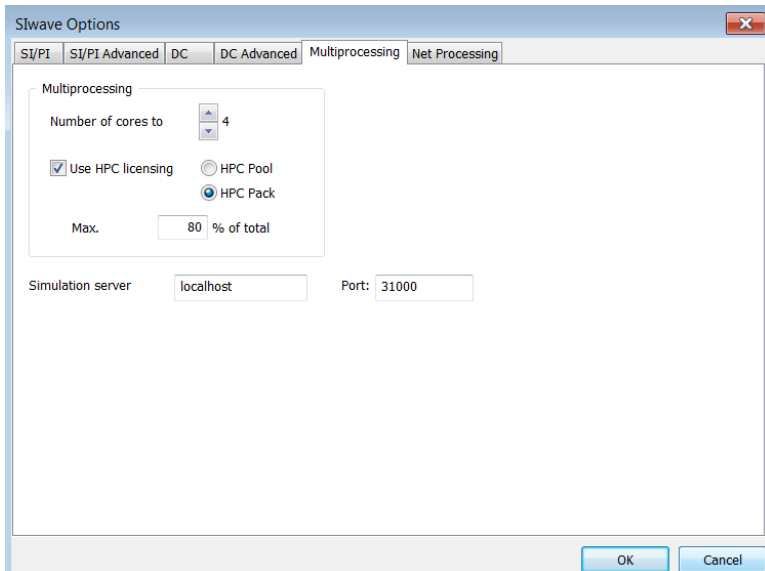


• Setting Simulation Global Options

- From the **Simulation** tab, Select **Options**

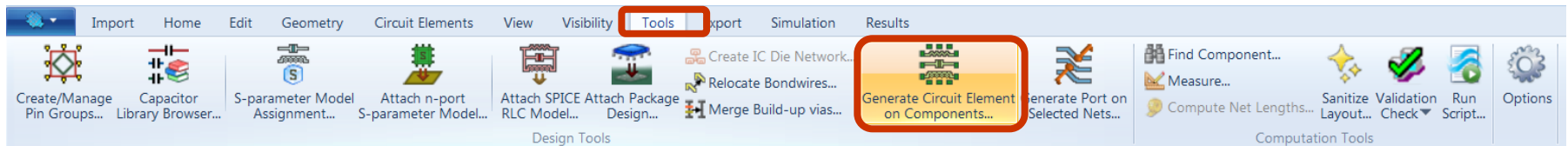


- Under **Multiprocessing** tab , set the number of cores you want to use
 - Check **Use HPC Licensing** to **HPC Pack** or **HPC Pool** if you have HPC licenses
- Under **Net Processing** tab
 - Ignore nets named “DUMMY” or “Unused” during Simulation: ☒ **Checked**
- Click **OK** button



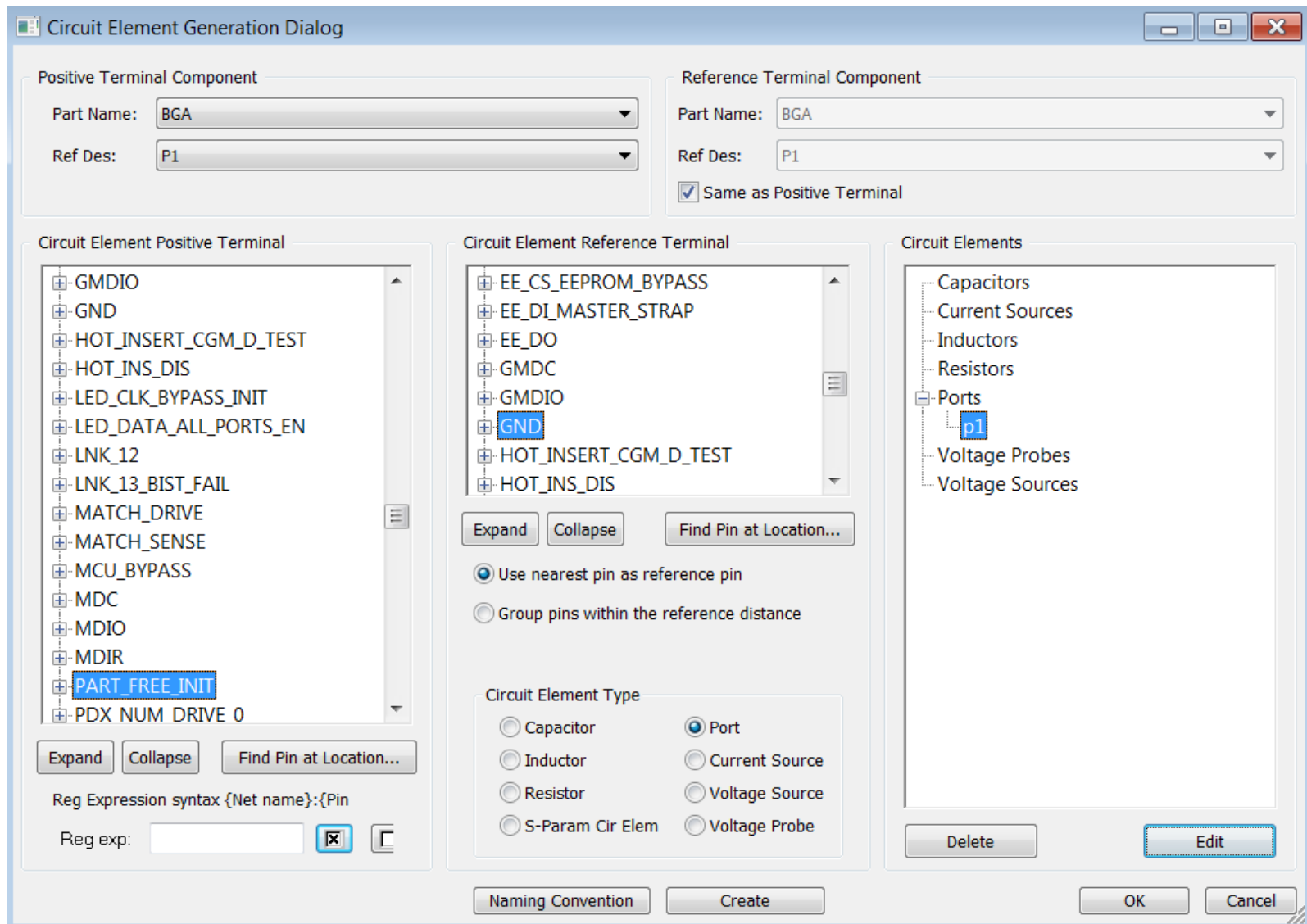
- **Define Ports on Signal Nets on the Solder Ball Side**

- To create port **P1** with the automatic port generation feature:
 - Go to the **Tools** tab, Select **Generate Circuits Element on Components...**



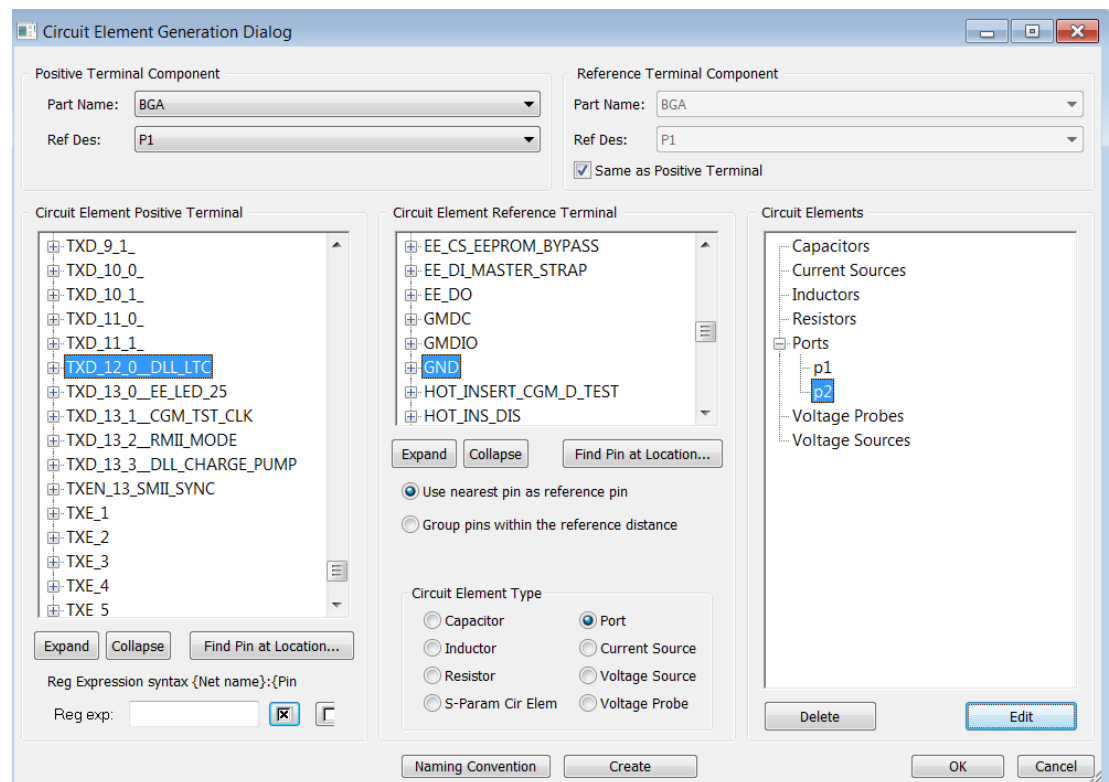
- Positive Terminal Component Part Name: **BGA**
- Positive Terminal Component Ref Des: **P1**
- Select the ☒ **Same as Positive Terminal**
- Select Circuit Element Positive Terminal: **PART_FREE_INIT**
- Select Circuit Element Reference Terminal: **GND**
 - Select option button for: **Use nearest pin as reference pin**
- Circuit Element Type: **Port**
- Click the **Create** button
 - Expand Ports under Circuit Elements column, you will see port PART_FREE_INIT_P1_D5 is listed there
 - Note: the default port naming convention is:
 <NETNAME>_<REFDES>_<POSTERMINAL>
- To rename the port:
 - Select **PART_FREE_INIT_P1_D5** from Ports in Circuit Elements
 - Click the **Edit** button
 - Name: **p1**
 - Click the **OK** button

Package S-parameters



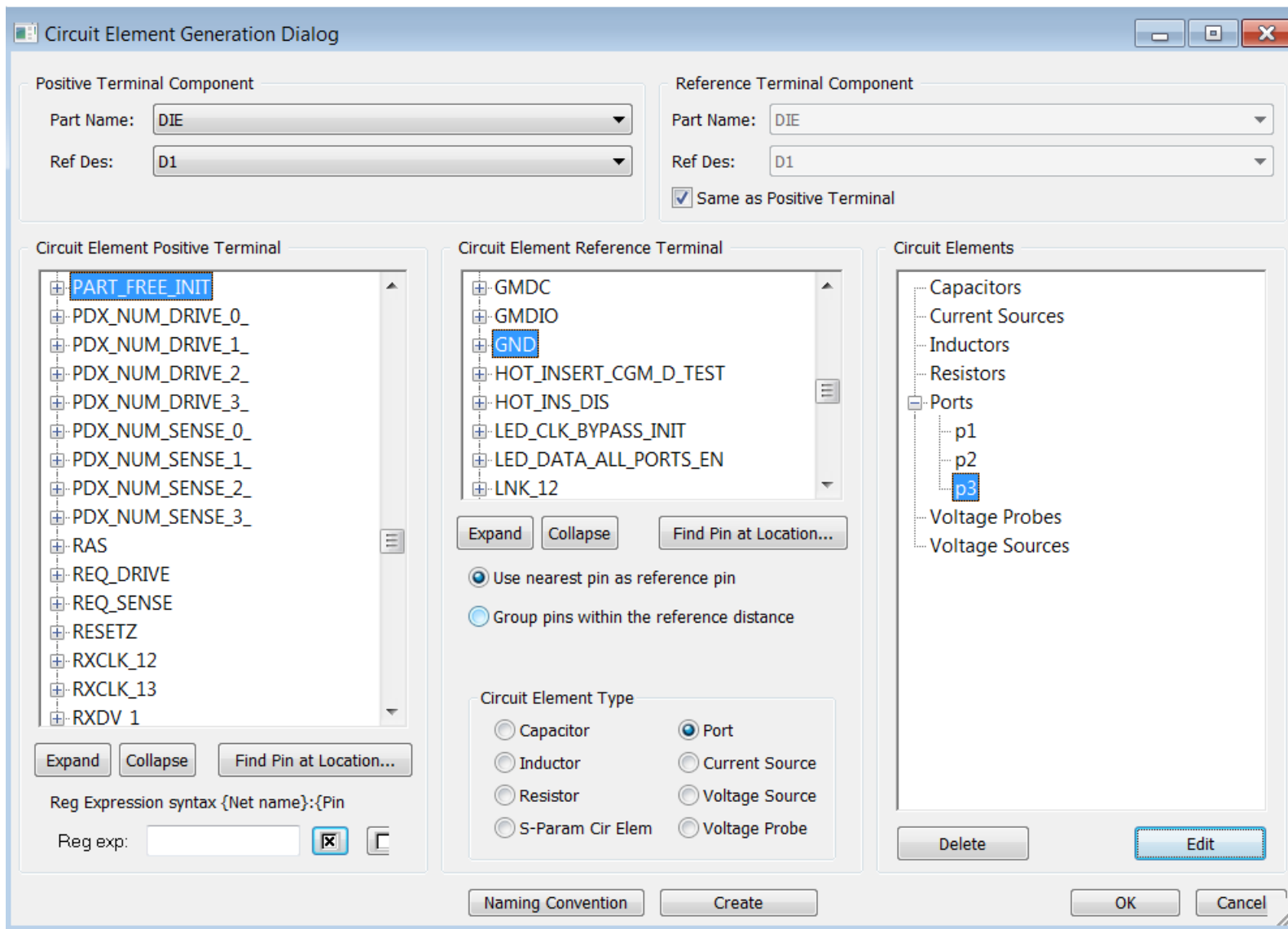
Package S-parameters

- To create port p2 with the automatic port generation feature:
 - Select in the Circuit Element Positive Terminal pane: **TXD_12_0__DLL_LTC**
 - Select in the Circuit Element Reference Terminal pane: **GND**
 - Select option button for: **Use nearest pin as reference pin**
 - Circuit Element Type: **Port**
 - Click the **Create** button
 - Select **TXD_12_0__DLL_LTC _P1_C4** under Ports in the Circuit Elements pane
 - Click the **Edit** button
 - Name: **p2**
 - Click the **OK** button



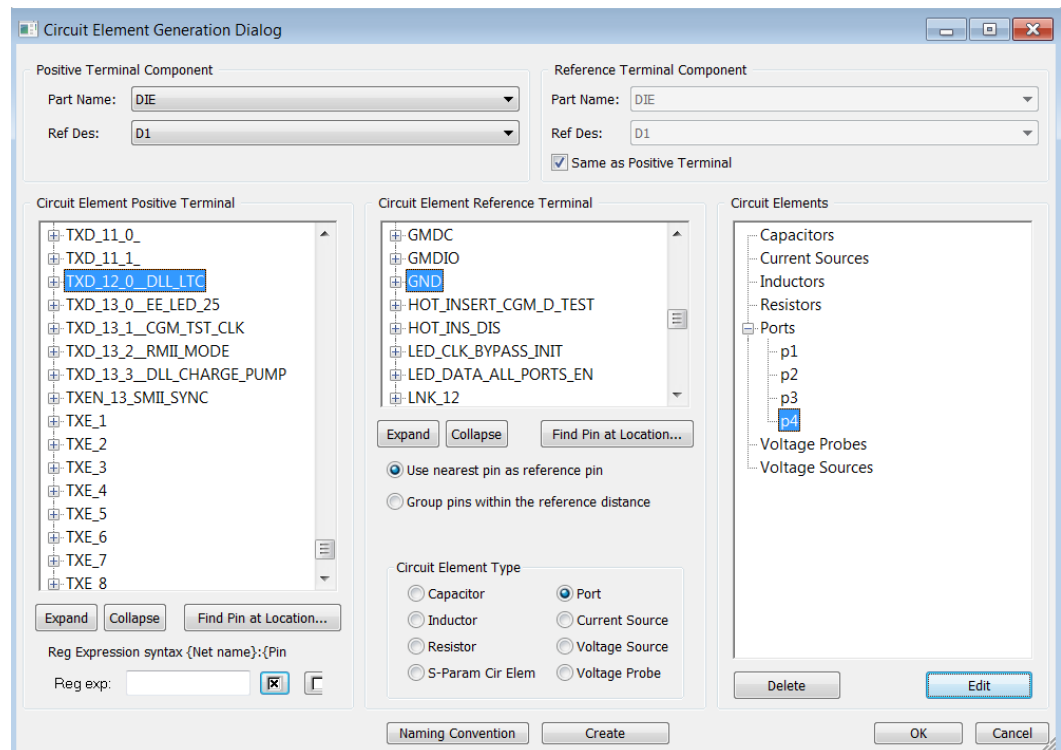
- **Define Ports on Signal Nets on the Bond Wire Side**
 - To create port p3 with the automatic port generation feature:
 - Positive Terminal Component Part Name: **DIE**
 - Positive Terminal Component Ref Des: **D1**
 - Select the ☒ **Same as Positive Terminal**
 - Select Circuit Element Positive Terminal: **PART_FREE_INIT**
 - Select Circuit Element Reference Terminal: **GND**
 - Select option button for: **Use nearest pin as reference pin**
 - Circuit Element Type: **Port**
 - Click the **Create** button
 - Select **PART_FREE_INIT_D1_290** from Ports in Circuit Elements
 - Click the **Edit** button
 - Name: **p3**
 - Click the **OK** button

Package S-parameters



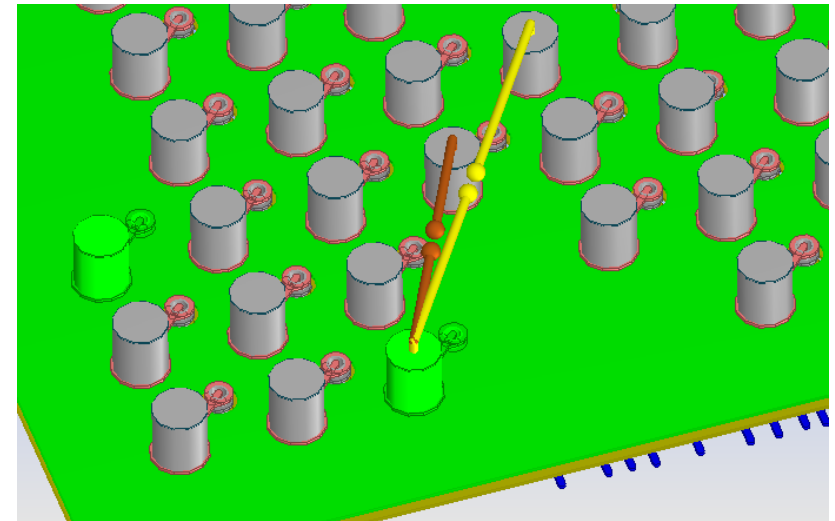
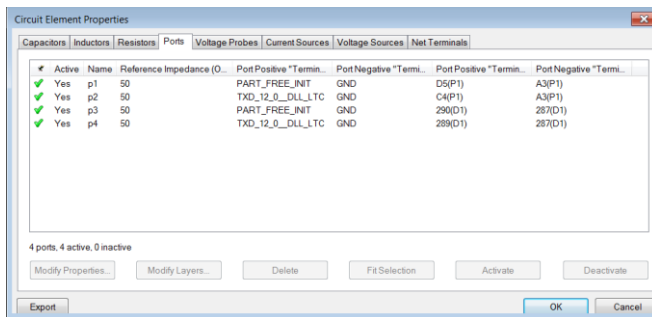
Package S-parameters

- To create port p4 with the automatic port generation feature:
 - Select in the Circuit Element Positive Terminal pane: **TXD_12_0__DLL_LTC**
 - Select in the Circuit Element Reference Terminal pane: **GND**
 - Select option button for: **Use nearest pin as reference pin**
 - Circuit Element Type: **Port**
 - Click the **Create** button
 - To rename the port:
 - Select **TXD_12_0__DLL_LTC _D1_289** under Ports in the Circuit Elements pane
 - Click the **Edit** button
 - Name: **p4**
 - Click the **OK** button
- Click the **OK** button



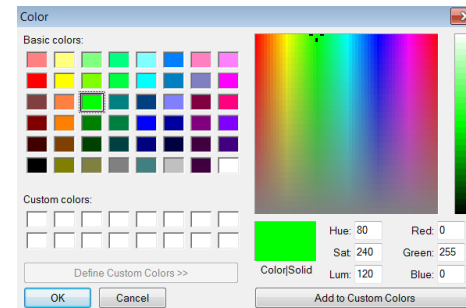
• Verify Ports

- Go the **Home** tab, select **Circuit Element Parameters**
- Activate the Ports tab
 - Click **OK** to exit.



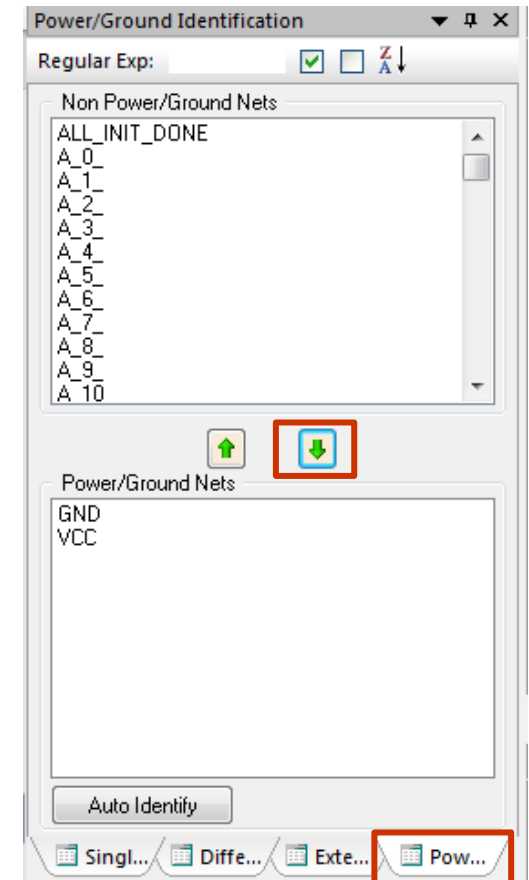
• View Ports Graphically

- Rotate the layout to have solder balls face up.
- Zoom in to the region where ports p1 and p2 are defined.
- To toggle off the simplify circuit elements display.
 - Go the **View** tab, Uncheck the item **Simplify Circuit Elements**
- To change the color of GND net so that the negative reference pin can be easily identified
 - Click the **Nets** tab
 - Highlight net **GND**
 - Right mouse click and select **Change Net Color**
 - Click on a green color from the color template, and click **OK**



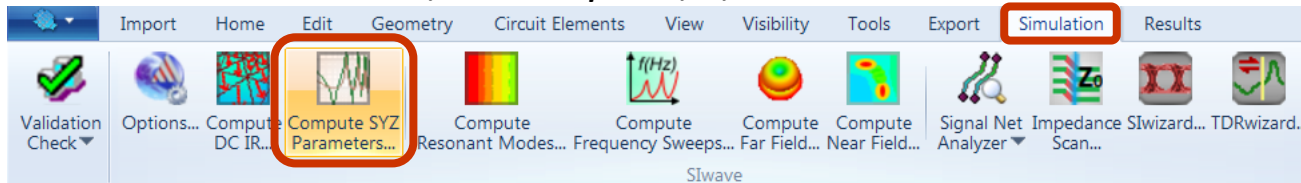
- **Defining Power and Ground Nets**

- The project in SIwave does not have the Power and Ground nets defined. To provide optimal simulation run time and accuracy the power and ground nets need to be configured.
- Navigate to the **Power/Ground Identification Workspace** in the side bars.
 - Scroll through the list of nets and find the net **GND** and select it by clicking on it.
 - Press the green down arrow to define the **GND** net as a power/ground net.
 - Repeat the process for the net labeled **VCC**.

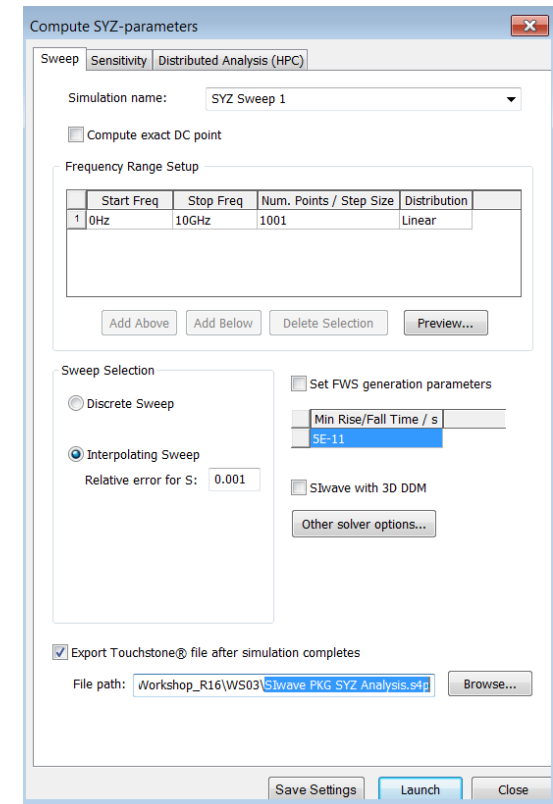
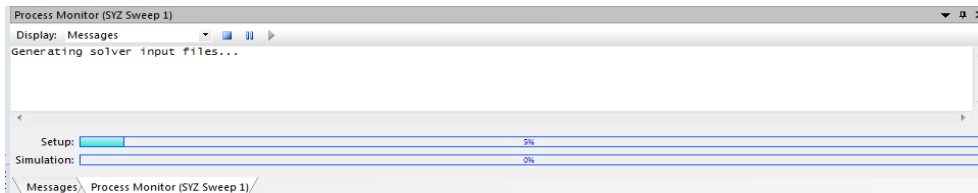


• Computing S-Parameters

- Form the menu **Simulation**, select **Compute S-, Y-, Z-Parameters...**



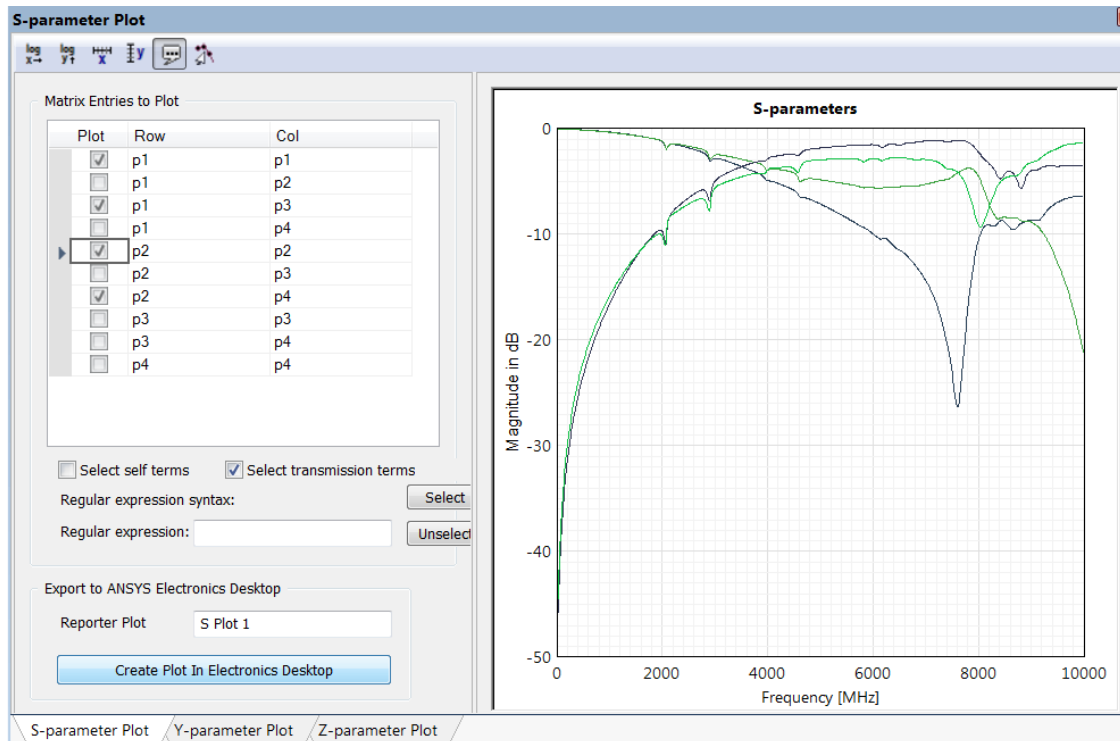
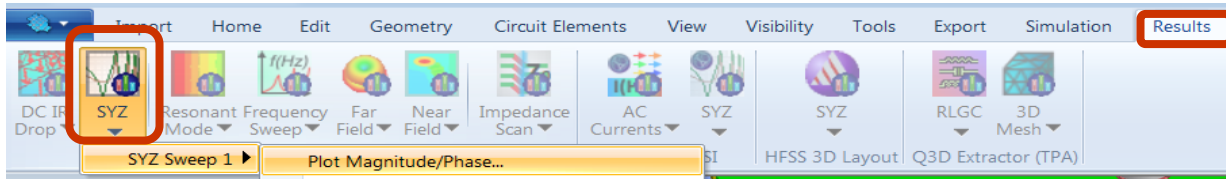
- Change the settings as shown below:
 - Start Freq: **0 Hz** and Stop Freq: **10 GHz**
 - Num. Points: **1001** and Distribution: **Linear**
 - Sweep Selection:
 - Option button: **Interpolating Sweep**
 - Error Tolerance: **0.001**
 - Check **Export Touchstone file after simulation completes**
- Click the **Launch** button to start the simulation
- Wait for the simulation to complete



Package S-parameters

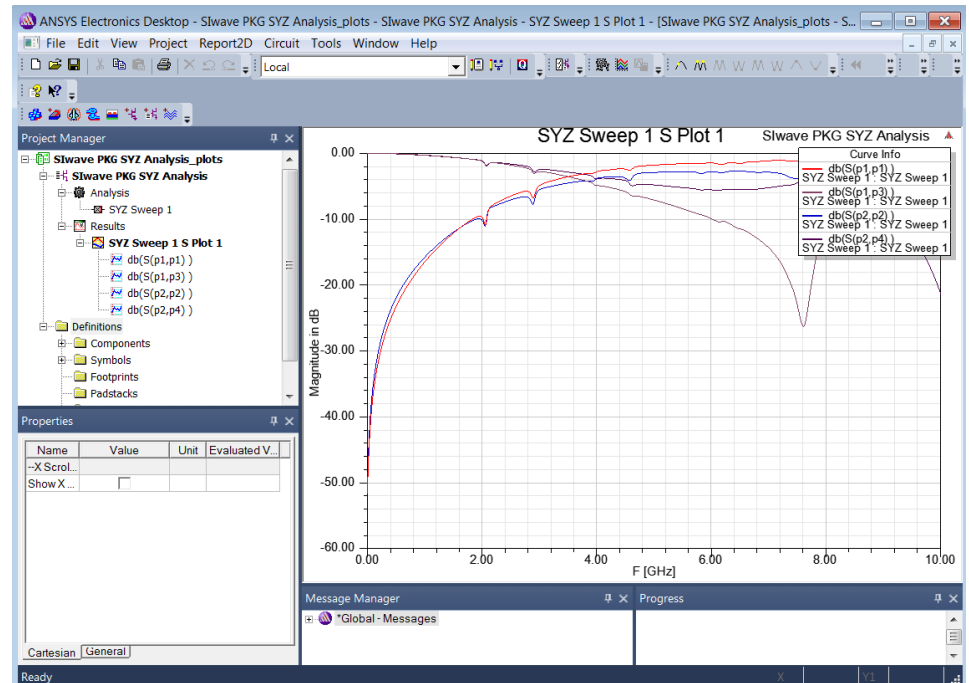
- **Open Report Editor**

- Go to the menu item **Results**, Select **SYZ** > **SYZ Sweep 1** > **Plot Magnitude/Phase...**



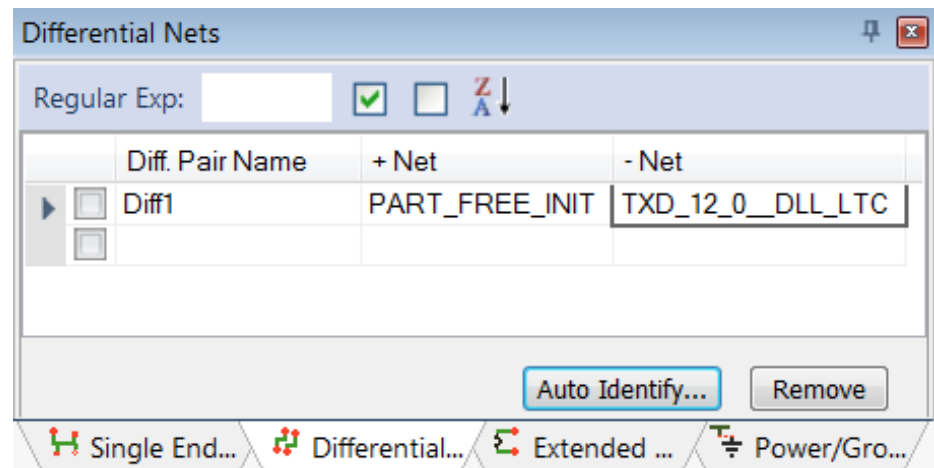
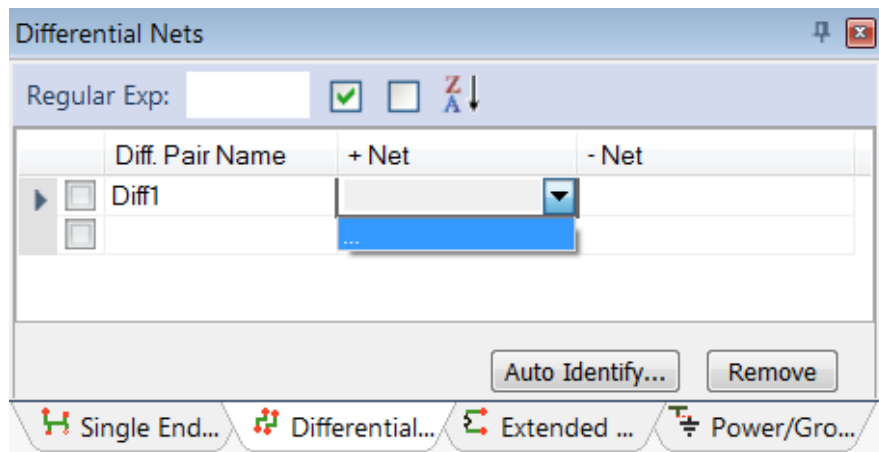
• Create New Plot in Electronics Desktop (Alternative)

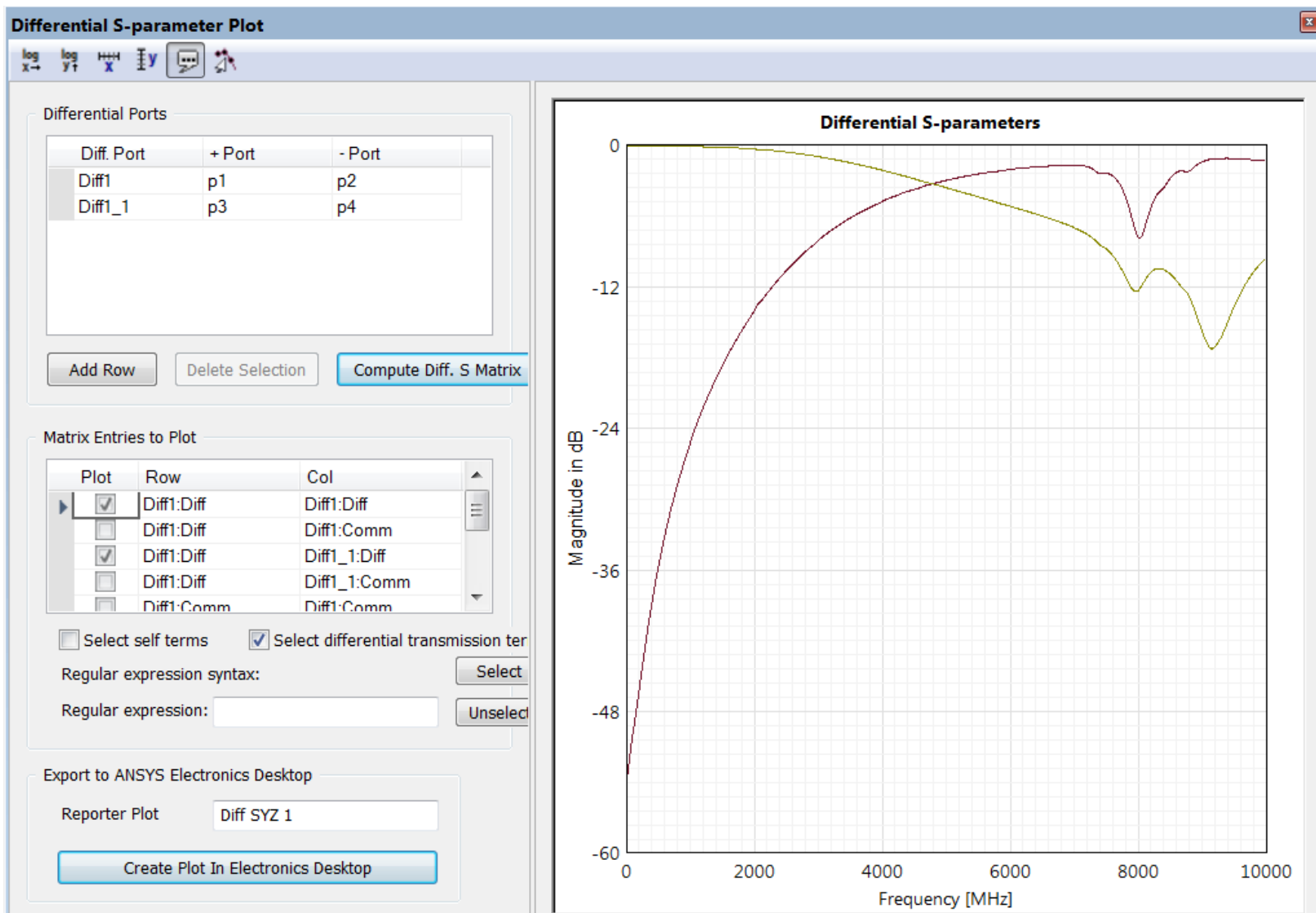
- In the SYZ Parameter Plot Generation window, place check marks next to (row, col):
 - p1,p1
 - p1,p3
 - p2,p2
 - p2,p4
- Click the **Create Plot In Electronics Desktop** button
 - These are the insertion and return losses from the die side for nets PART_FREE_INIT and TXD_12_0__DLL_LTC
- When done viewing the S-Parameters, select the menu item **File > Exit**
 - Click the **Yes** button to save the changes if prompted
- Close the S-parameter Plot dialog



• Compute Differential S-parameters

- Nets `PART_FREE_INIT` and `TXD_12_0__DLL_LTC` are not a differential pair, but let's assume they are for the purpose of demonstrating how to obtain differential S-parameters
- To compute differential S-parameters:
 - Activate the Differential Nets workspace in the sidebar by activating the **Differential Nets** tab.
 - Note:** If the **Differential Nets** is not present make sure that **Views > Workspaces > Differential Nets** is checked.
 - Diff. Pair Name: **Diff1**
 - + Net: click ... in the end of the pull down list and select **PART_FREE_INIT**
 - - Net: select **TXD_12_0__DLL_LTC** from the pull down list
 - Go to **Results** tab and Select > **SYZ > SYZ Sweep 1 > Compute Differential S-Parameters**
 - Click the **Compute Diff. S Matrix** button
 - In the Matrix Entries to Plot pane select **(Diff1:Diff, Diff1:Diff)** and **(Diff1:Diff, Diff1_1:Diff)** and compare with the results shown on the next slide
 - Close the **Differential S-parameter Plot** dialog



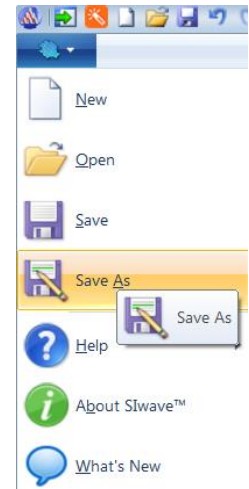
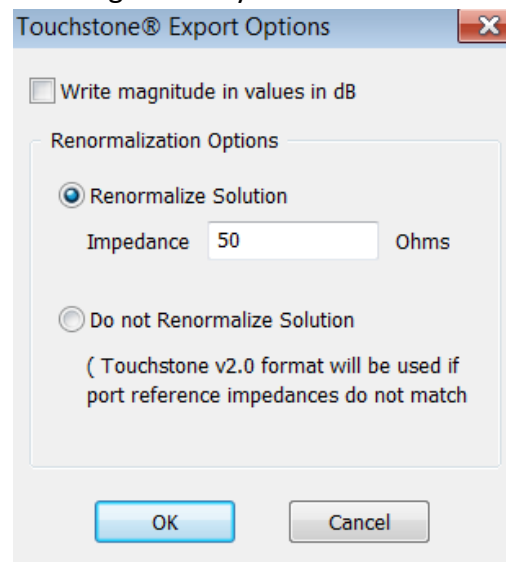
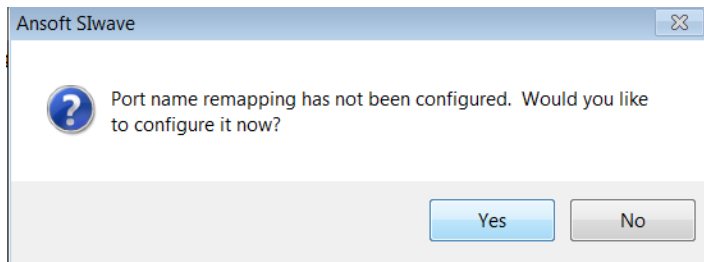


• Save SIwave Project

- From the main menu, Select **Save As**
 - Filename: **bga_s-para**
 - Click the **Save** button

• Export Touchstone File

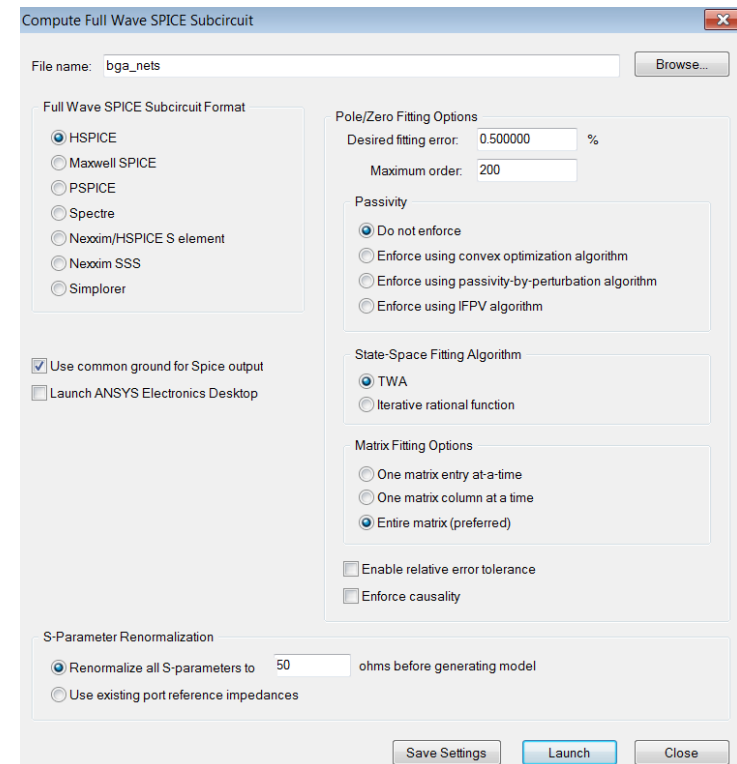
- From the **Results** tab, Select **SYZ > SYZ Sweep 1 > Export to Touchstone® File...**
 - Filename: **bga_s-para**
 - Click the **Save** button
 - Click the **No** to not configure the Port Name remapping now
 - Click the **OK** to accept the 50 ohms renormalization
 - Touchstone file **bga_s-para.s4p** is created in the working directory



Package S-parameters

• Creating a Full Wave Spice Subcircuit

- From the **Results** tab , Select **SYZ > SYZ Sweep 1 > Compute FWS sub-circuit**
 - File name: **bga_nets**
 - By default the file will be saved in the project directory
 - Full Wave SPICE Subcircuit Format: **HSPICE**
 - Use common ground for Spice output: ☒ **Checked**
 - Click the **OK** button
 - The HSPICE subcircuit bga_nets.sp is created in the project directory



Package S-parameters

• Creating a Lumped RLGC Subcircuit

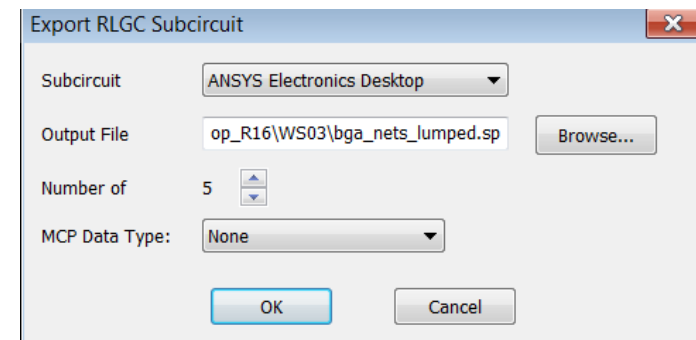
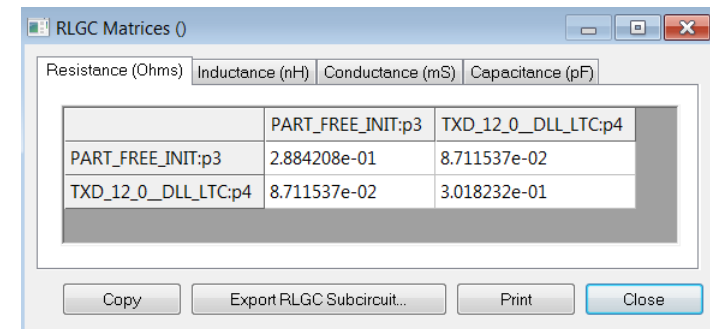
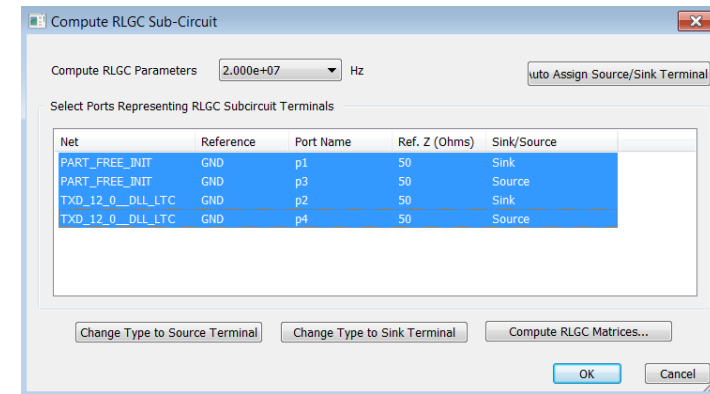
- From the **Results** tab, Select **SYZ > SYZ Sweep 1 > Compute RLGC sub-circuit...**
 - Compute RLGC Parameters at: **2.000e+07Hz (or closest in the list)**
 - Click the **Auto Assign Source/Sink Terminals** button
 - Select all items in the table listing
 - Click the **Compute RLGC Matrices** button
 - A window as shown below will come up
 - Activate the tabs to see R, L, G, or C matrix
- To create a lumped RLGC subcircuit:
 - Click the **Export RLGC Subcircuit** button
 - Subcircuit Format: **HSPICE**
 - Output File Name: **bga_nets_lumped**
 - Number of Lumps: **5**
 - Click the **OK** button
 - Lumped subcircuit bga_nets_lumped.sp is created
 - Click the **Close** button on the RLGC Matrices dialog
- Click the **OK** button to exit Compute RLGC Sub-Circuit dialog

• Save Slwave Project

- From the main menu, Select **Save**

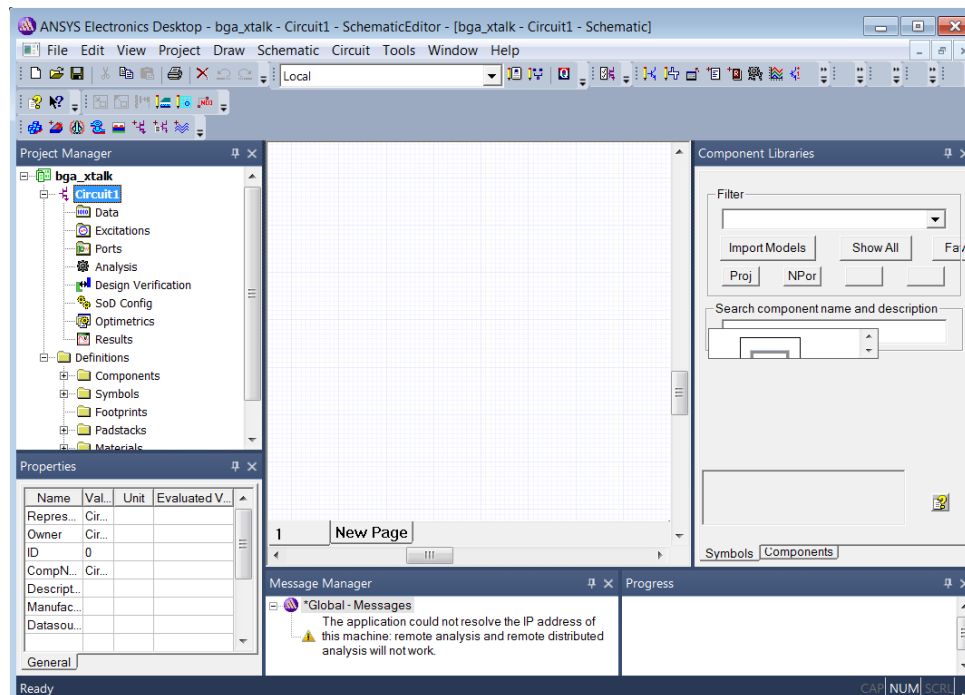
• Exit Slwave

- From the main menu, Select **Exit**

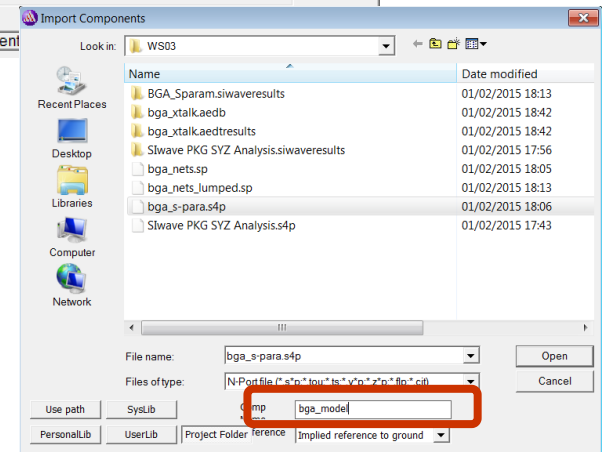
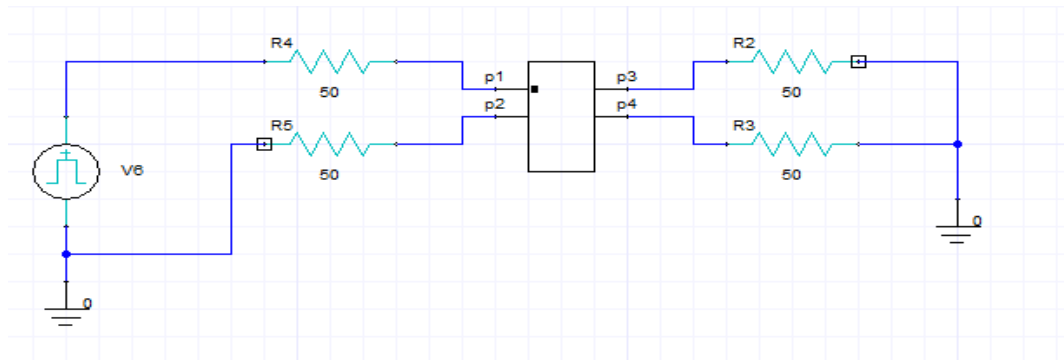


Crosstalk Circuit Simulation

- **Launching ANSYS Electronics Desktop**
 - To launch ANSYS Designer select:
 - All Programs > ANSYS Electromagnetics > ANSYS Electromagnetics Suite 16.0 > ANSYS Electronics Desktop 2015
- **Creating a New Circuit**
 - Select the menu item **Project > Insert Circuit Design**
 - Select the menu item **File > Save As**
 - Save the project to a convenient location using the name **bga_xtalk**



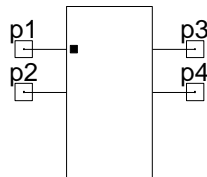
- From the **Component Libraries** window on the right
 - Click on **Import Models** button and Select **Nport** using the slider bar
 - In the **Import Components** data window,
 - Select the Filename: **bga_s-para.s4p**
 - Comp Name: **bga_model**
 - Accept the default selection: **Implied reference to ground**
 - Click the **Open** button
 - Place the S-parameter file into the schematic
 - Press **ESC** key to end component placement mode



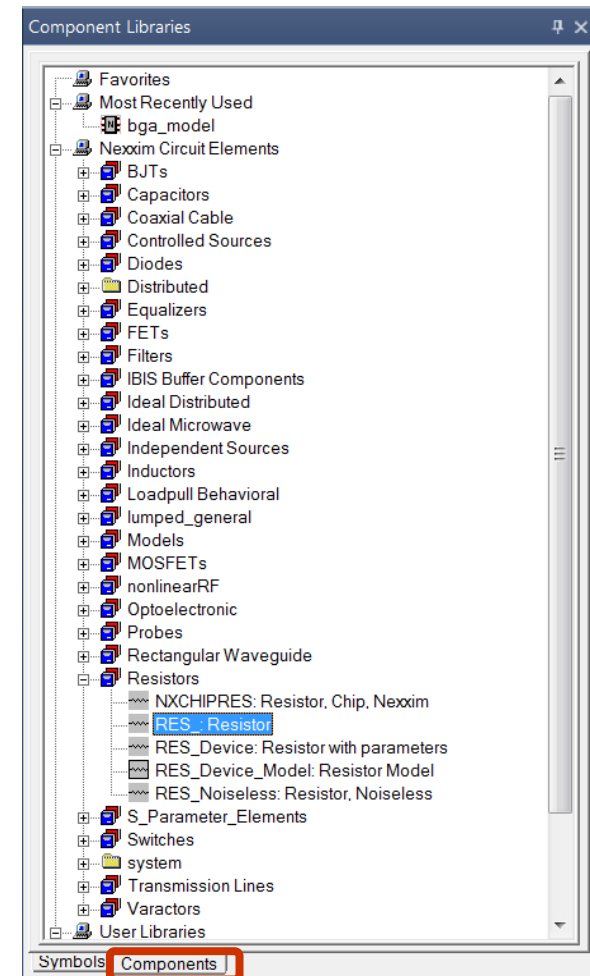
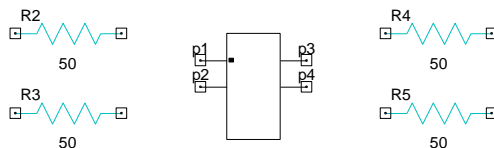
Package S-parameters

• Component Placement – continued

- Placing resistors, voltage sources, and voltage probes:
 - Select the following components from the **Components** tab
 - Resistors : expand **Resistors**
 - Voltage sources: expand **Independent Sources**
 - Voltage probes: expand **Probes**

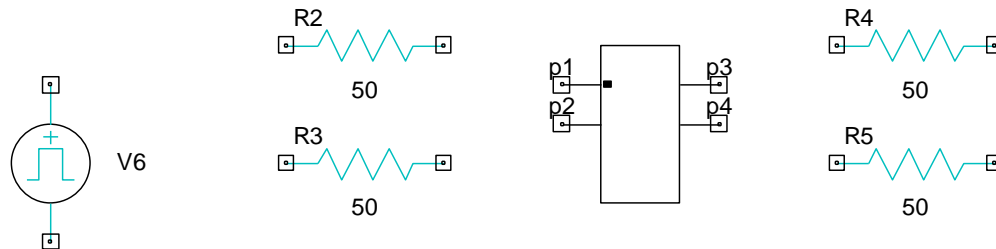


- Place four Resistors in the schematic
 - In the Components tab, under **Resistors**, double click **RES_: Resistor**
 - Click the left mouse button to place resistors in the schematic
 - To end the placement, click the right mouse button and select Finish. You can also end the placement by pressing the space bar or **ESC** keys on the keyboard.



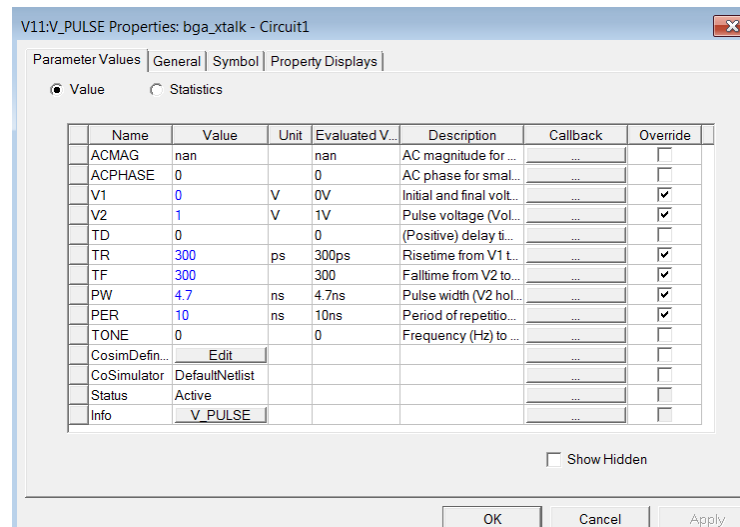
• Component Placement – continued

- In the Components tab under **Independent Sources** double click on **V_PULSE: Pulse Voltage Source**
 - Left mouse click to place the source in the schematic
 - Press the space bar to finish the placement



• Define Pulse Source

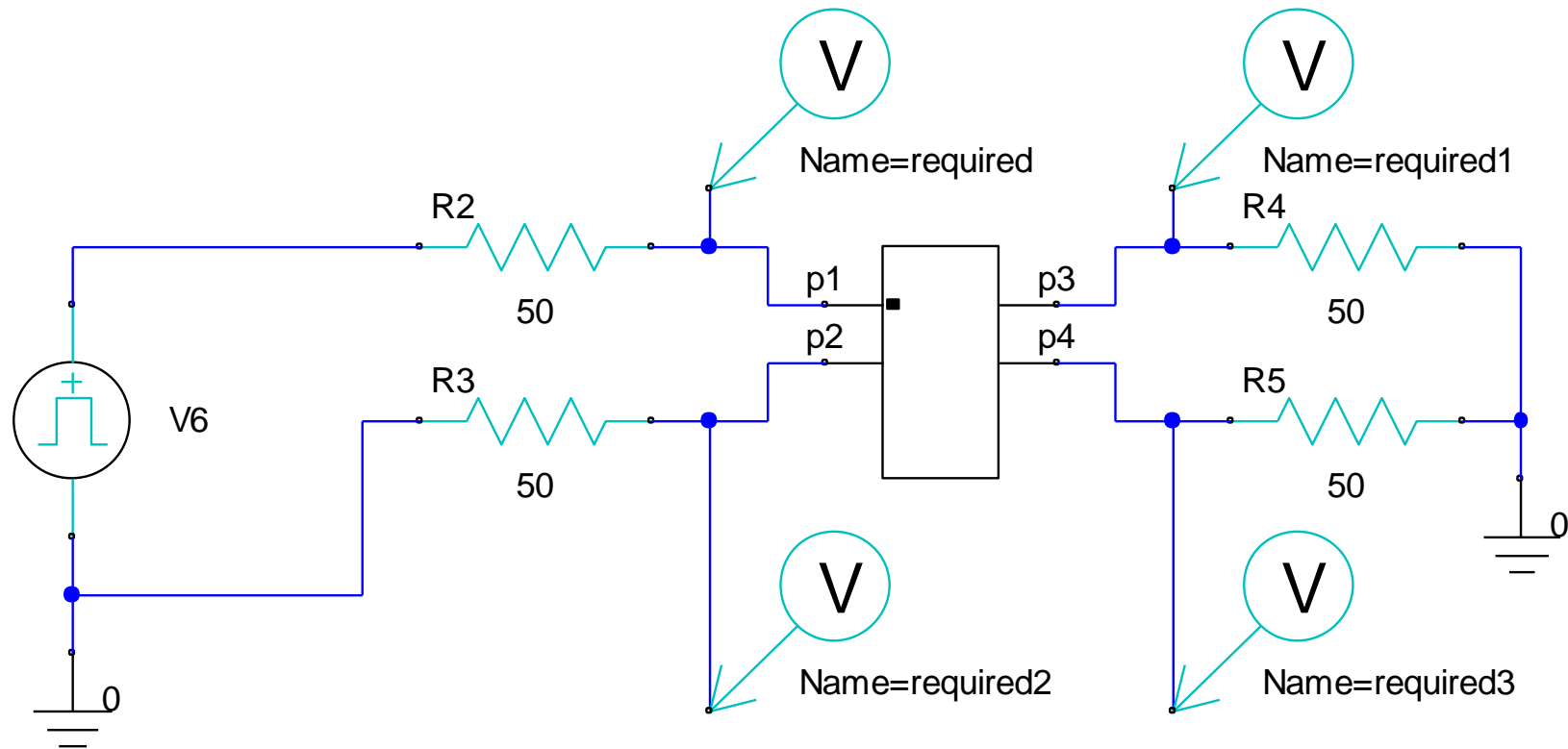
- Right mouse click the source component and then select Properties in the pull down menu
- Enter the pulse properties as show below
 - V1: 0 V**
 - V2: 1 V**
 - TR: 300 ps**
 - TF: 300 ps**
 - PW: 4.7 ns**
 - PER: 10 ns**
- Click the **OK** button



- **Component Placement – continued**

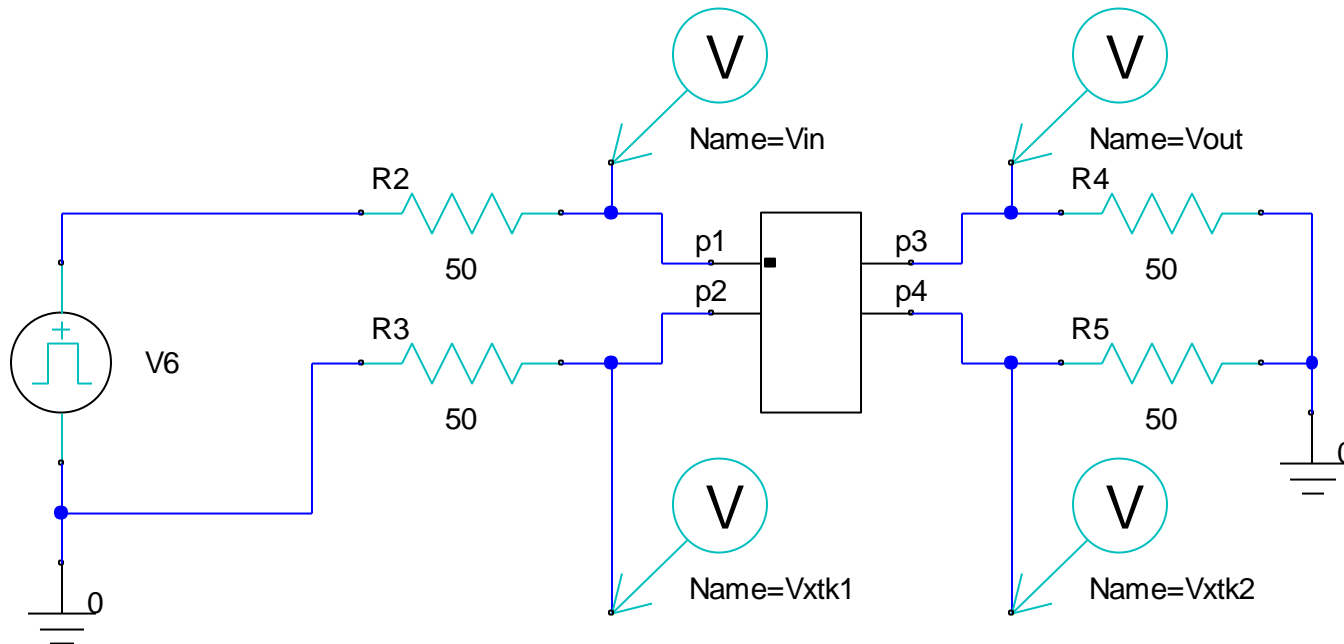
- Adding Ground Connections
 - Select the menu item **Draw > Ground** (alternatively you can select the toolbar icon)
 - Place one ground connection on each of the left and right sides of the circuit as shown on the next page
- Adding Wiring to connect components
 - Place the cursor over a node (it will change to an X shape) and click the left mouse button once
 - Move the mouse to another node and click the left mouse button once to create a wire between the nodes
 - Repeat this procedure until the connections shown on the next page are made
- Adding Voltage Probes Points
 - In the Components tab under **Probes** double-click on **VPROBE: Voltage Probe**
 - Left-click on the wire connecting port **p1** on the S-parameter component and resistor **R1**
 - Left-click to place additional voltage probes on each of the other wires attached to the S-parameter component
 - You can click and drag the voltage away from their original locations to prevent them from overlapping with other display elements

Package S-parameters



• Component Placement – continued

- Double-click the voltage probe connecting the **R2** resistor to port **p1** to open its Properties window
 - Enter Name: **Vin**
- Double-click the voltage probe connecting the **R4** resistor to port **p3** to open its Properties window
 - Enter Name: **Vout**
- Double-click the voltage probe connecting the **R3** resistor to port **p2** to open its Properties window
 - Enter Name: **Vxtk1**
- Double-click the voltage probe connecting the **R5** resistor to port **p4** to open its Properties window
 - Enter Name: **Vxtk2**



Package S-parameters

- **Save Project**

- In the ANSYS Electronics Desktop window, select the menu item **File > Save**

- **Analysis Setup**

- Select the menu item **Circuit > Add Nexxim Solution Setup... > Transient Analysis**
 - Analysis Control
 - Step: **0.1ns**
 - Stop: **20ns**
 - Click the **OK** button
- Select the menu item **Circuit > Analyze**

Transient Analysis

Name: ☐ Disable

Analysis Control

Step: ns

Stop: ns

Accuracy:

Output Quantities

Sweep Variables

| Name | Sweep/Value |
|------|-------------|
| | |

☐ Enable Transient Noise

Noise fmax: Noise Scale: Noise Seed: ☐ Enable multiple runs

Noise fmin: Runs:

Solution Option

Name:

Additional:

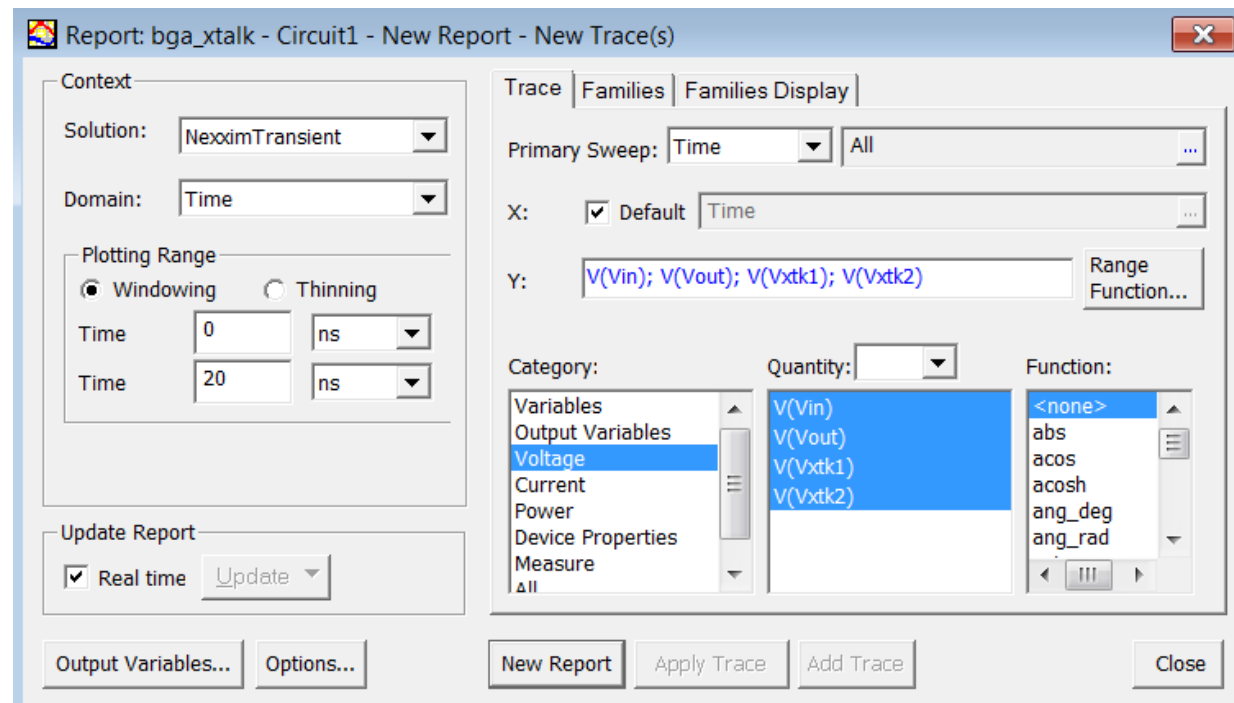
- **Plot Input, Output and Crosstalk Waveforms**

- Select the menu item:

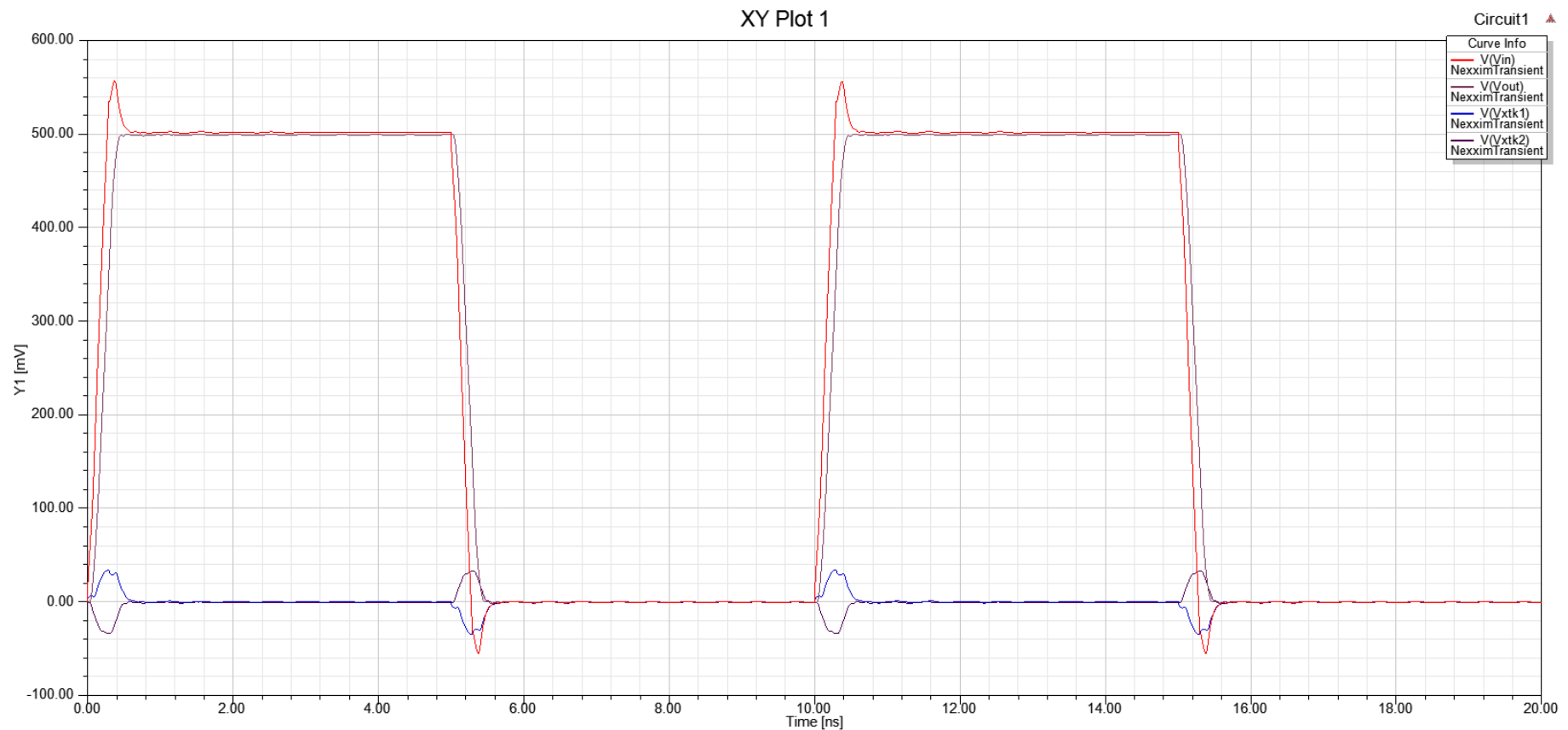
Circuit > Results > Create Standard Report > Rectangular Plot

- New Traces Window:

- Category: **Voltage**
- Quantity: **V(Vin), V(Vout), V(VxTk1), V(VxTk2)**
- Function: **<none>**
- Click the **New Report** button
- Click the **Close** button



Package: Transient waveforms



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