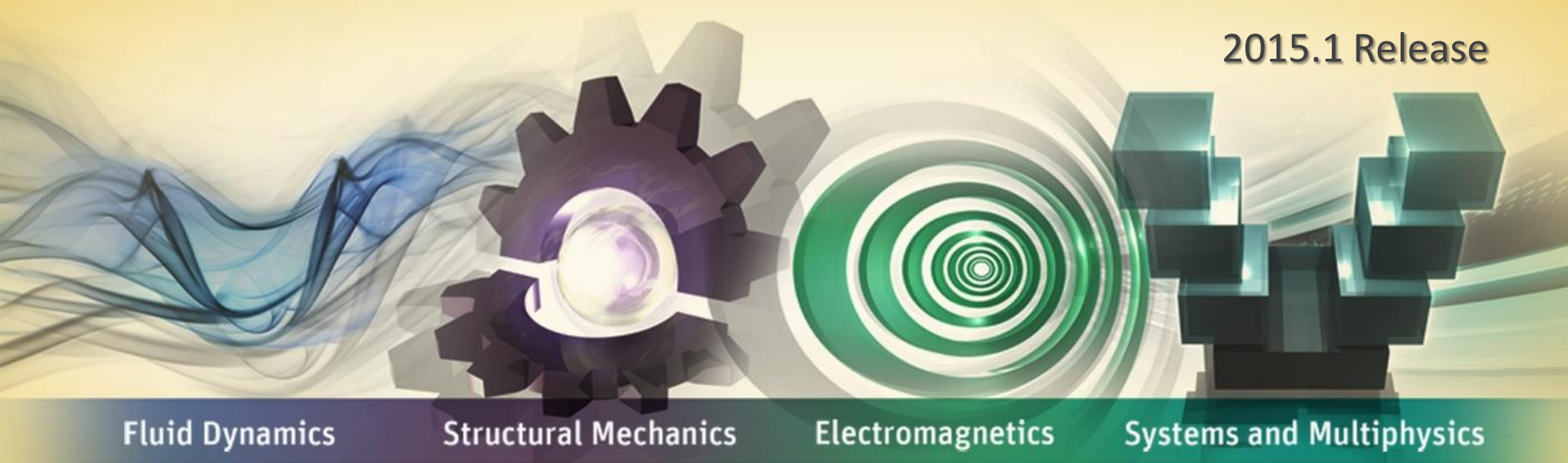


Workshop 2: Validation Checker

2015.1 Release



Introduction to ANSYS SIwave

SIwave Validation Checking Example

- **Validating Imported Design**

- With all simulations it is important to verify that the geometry is represented as expected. CAD engineers often leave incorrect or missing information in layout. Often intermediate revisions of boards can lack complete information as well. Failure to validate can lead to unexpected results and discrepancies with fabricated hardware. In this example we will describe in detail the step by step procedure to ensure your imported geometry is correct.

- **Validation Procedure Overview**

- Review warnings
- Visually inspect geometry
- Check stackup
- Run Validation Check
- Examine components
- Examine padstacks

- **Review Warnings**

- When you first import a design into SIwave, any potential abnormalities will be listed in the message window. It is important to review this warnings and verify that they are benign.

- Open ANSYS SIwave:

All Programs > ANSYS Electromagnetics > ANSYS Electromagnetics Suite 16.0 > ANSYS SIwave 2015

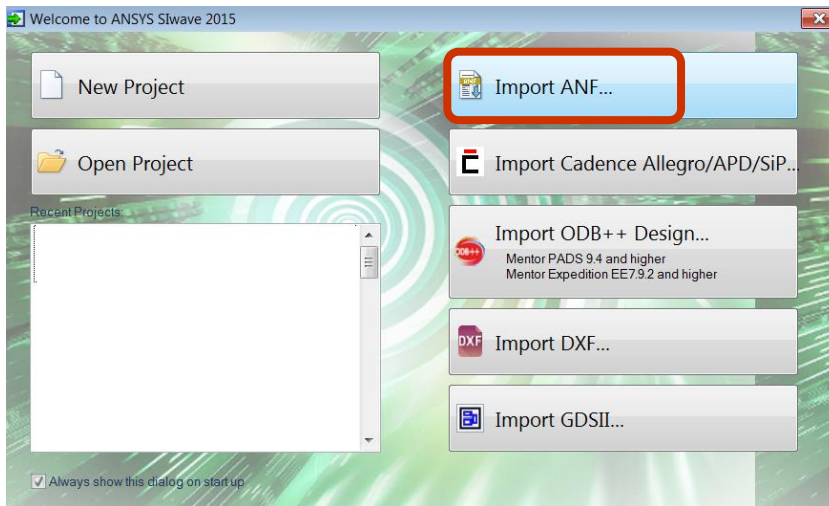
- Select the menu item **File > Import > ANF...**
 - Navigate to the training files and choose: **Validation_Check.anf**
- Select the menu item **File > Import > Component File...**
 - Navigate to the training files and choose: **Validation_Check.cmp**
 - If there is a warning message click the **Yes to All** button to overwrite existing names
- **Notes:**

- If problems were discovered when parsing this geometry they would be listed in the Message Window.

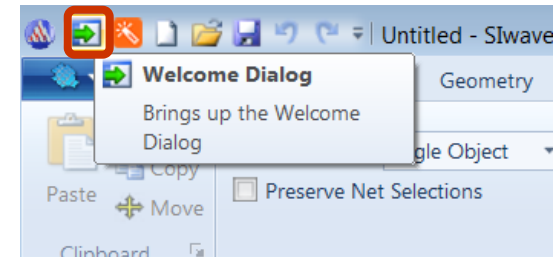
• Starting SIwave

- To launch SIwave, click the Microsoft **Start** Button, select: **All Programs > ANSYS Electromagnetics > ANSYS Electromagnetics Suite 16.1 > ANSYS SIwave 2015.1**

The Welcome Window will appear



Otherwise click on the Welcome Dialog Button

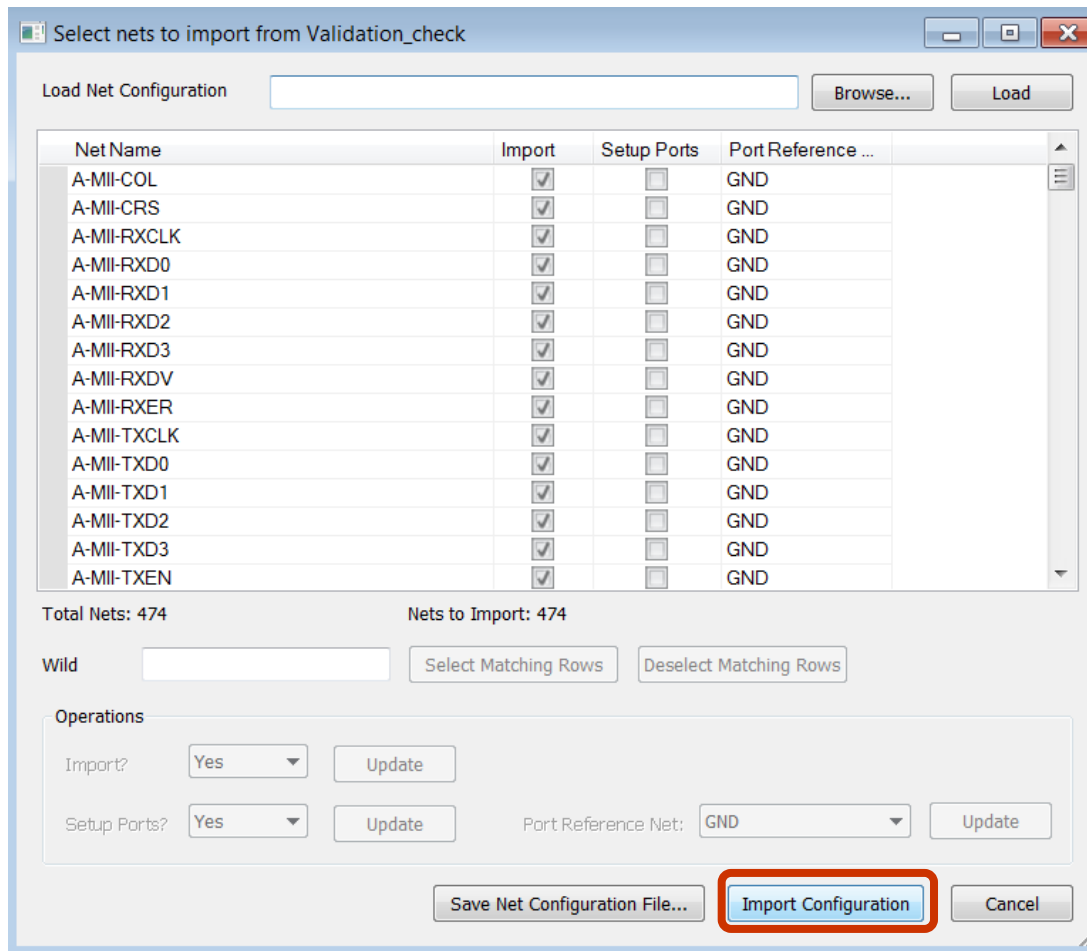


• Import the .ANF (Ansoft Neutral File) file

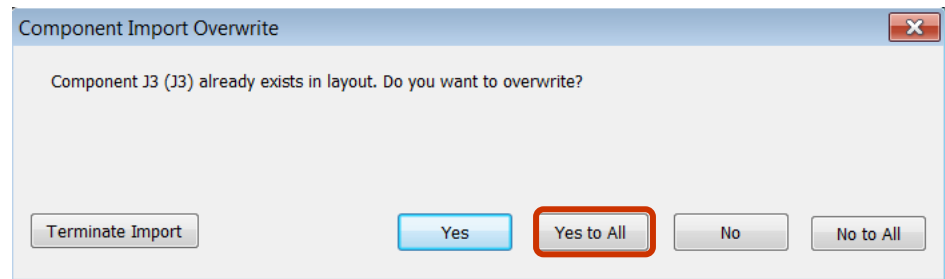
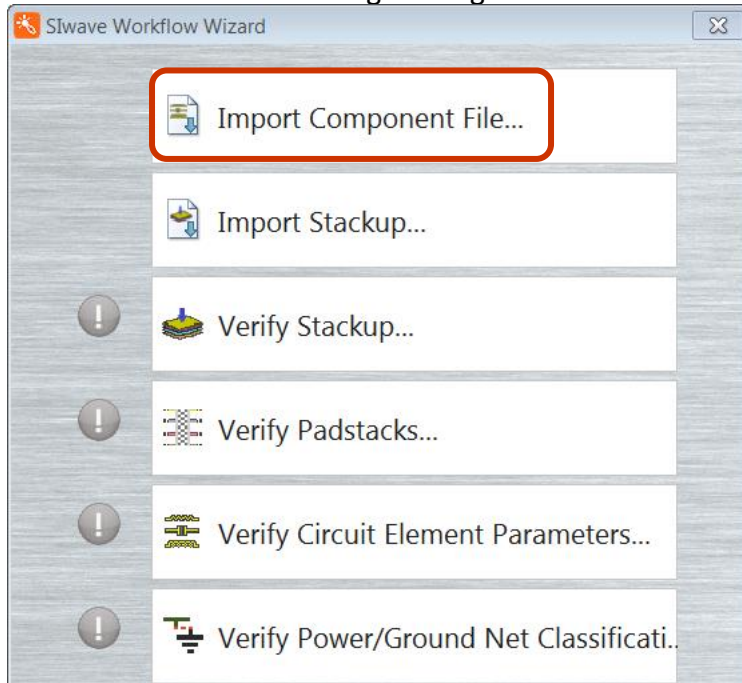
- Click the Import ANF... box
 - Navigate to the training files and choose : **Validation_check.anf**
 - Click the **Open** button

Validation Check

- The Select nets box will appear. (If desired, the user can filter nets to be imported. For this example, all nets will be imported)
- Click the **Import Configuration** button



- The SIwave Workflow Wizard will appear
- Import the .cmp (Ansoft Component File)
 - Click on the **Import Component File...** button
 - Navigate to the training files and choose : **Validation_check.cmp**
 - Click the **Open** button
 - If there is a warning message click the **Yes to All** button to overwrite existing names

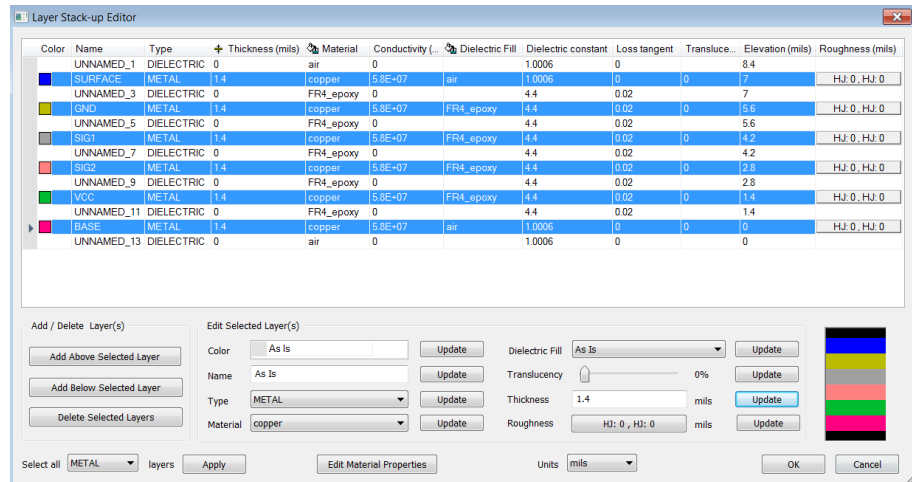
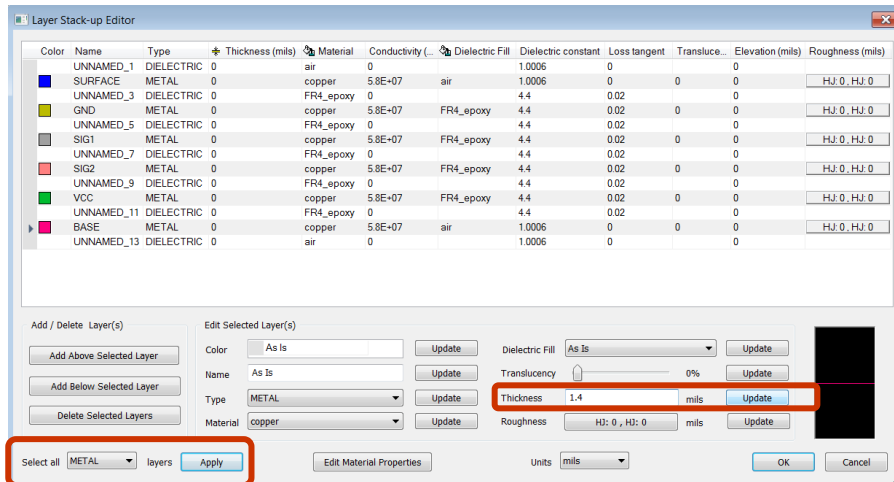
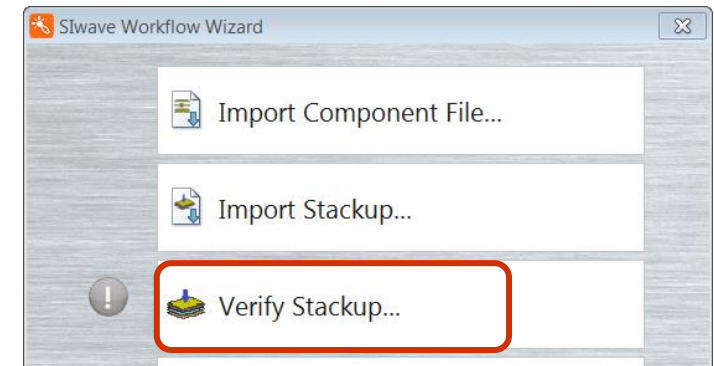


- **Notes:**
 - If problems were discovered when parsing this geometry they would be listed in the Message Window.

Validation Check

• Check Stackup

- Layer dimensions and materials are often ignored by the layout engineer. After importing a design it's important to check the stackup for proper dimensions and material.
- From the Siwave Workflow Wizard dialog, click **Verify Stackup...**
 - Notice the layers are all zero thickness
 - Select all metal layers:
 - Use the **Select all METAL** in bottom left corner and **Apply**
 - Under menu **Edit Selected Layer**
 - Thickness : **1.4 mils**
 - Click the **Update** button



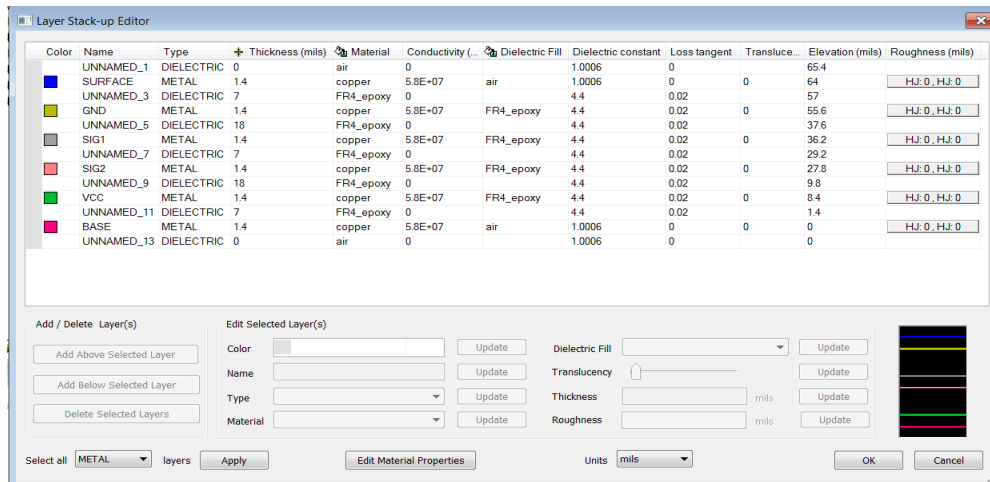
Validation Check

• Check Stackup

- Hold **Ctrl** key down and select the dielectric layers:
 - **UNNAMED_3, UNNAMED_7 and UNNAMED_11**
- Under menu **Edit Selected Layer**
 - Thickness: **7 mils** and Click the **Update** button
- Hold **Ctrl** key down and select the dielectric layers:
 - **UNNAMED_5 and UNNAMED_9**
- Under menu **Edit Selected Layer**
 - Thickness: **18 mils** and Click the **Update** button
- The correct stackup is shown below
- Click the **OK** button to close the Layer Stack-up Editor

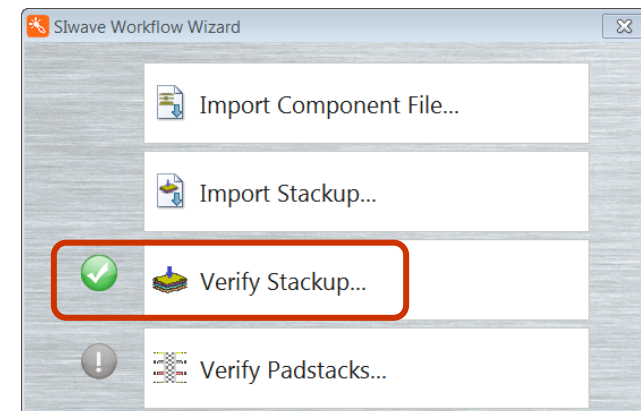
Click in gray to select layer.

Color	Name	Type
	UNNAMED_1	DIELECTRIC
	SURFACE	METAL
	UNNAMED_3	DIELECTRIC
	GND	METAL
	UNNAMED_5	DIELECTRIC
	SIG1	METAL
	UNNAMED_7	DIELECTRIC
	SIG2	METAL
	UNNAMED_9	DIELECTRIC
	VCC	METAL
	UNNAMED_11	DIELECTRIC
	BASE	METAL
	UNNAMED_13	DIELECTRIC



• Verify the Layer Stackup

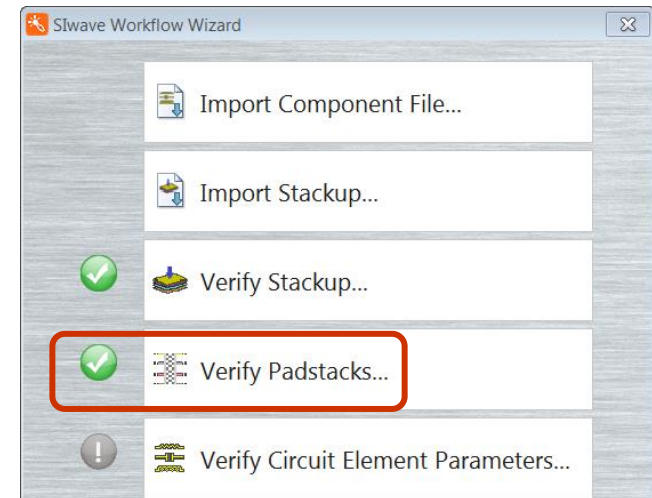
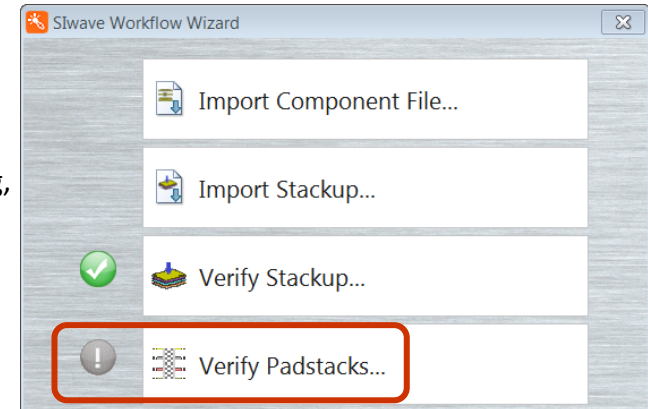
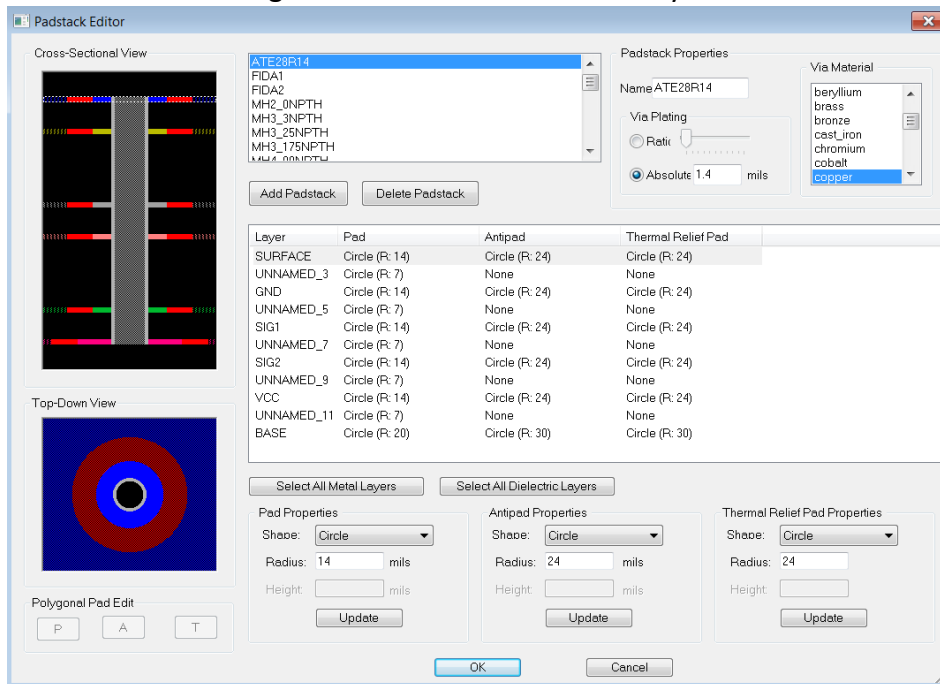
- There should be a green check mark next the to Verify Stackup



Validation Check

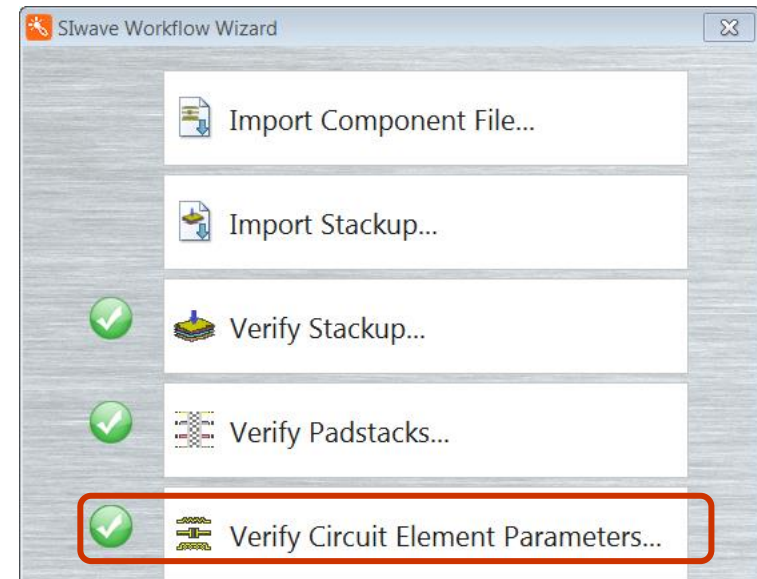
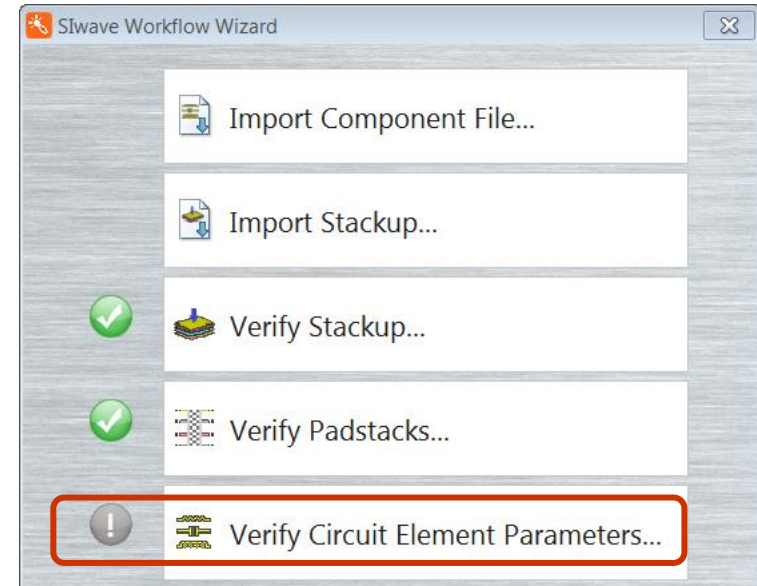
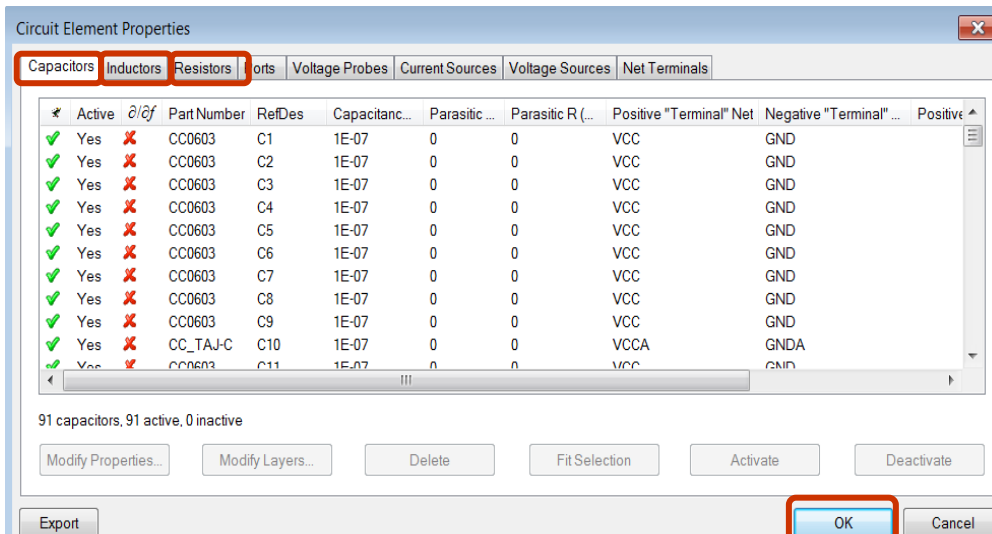
• Verify Padstacks

- Sometimes the padstacks are not properly defined within the layout tool and antipads may be missing. Ideally this should be corrected in layout before exporting, but the information may also be modified within SIwave
- Click on **Verify Padstacks...**
 - Scroll through the list of available padstacks
 - Note that through hole vias that have pads defined should also have antipads associated with them
 - After verifying click **OK** to close
- There should be a green check mark next to Verify Padstacks



Validation Check

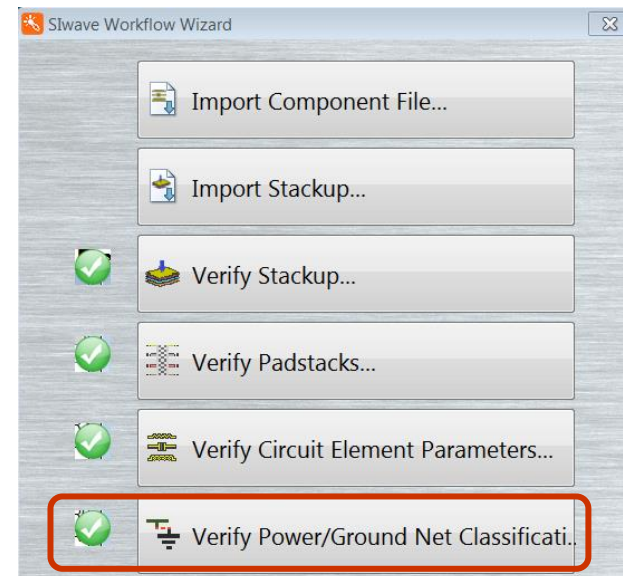
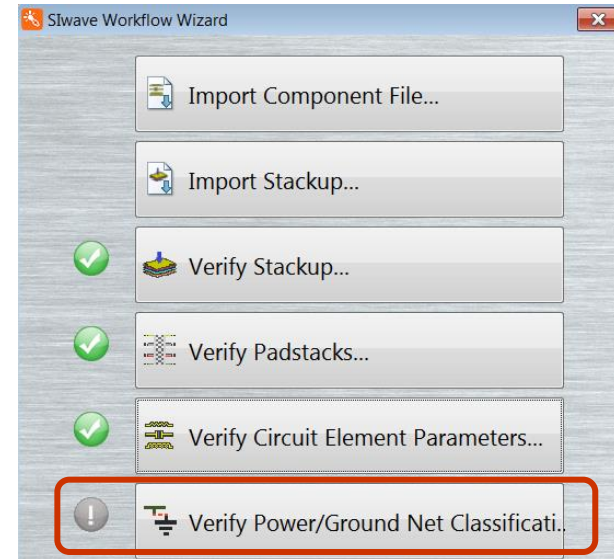
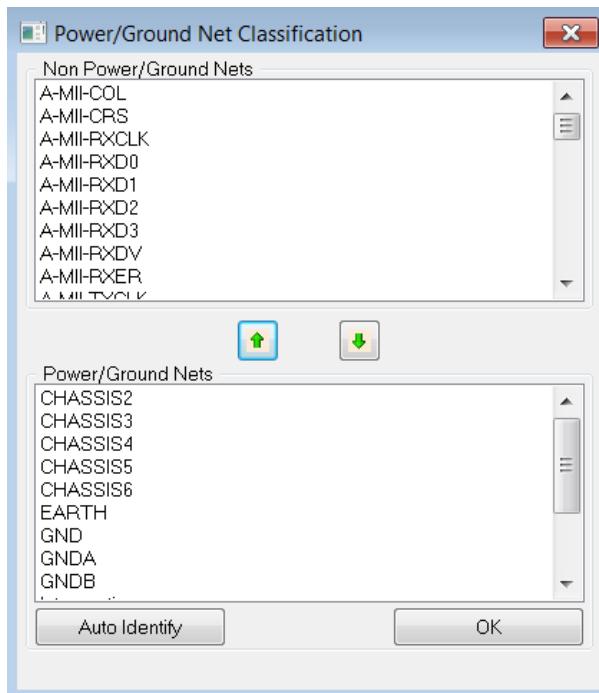
- **Verify and Reassign Circuit Element Parameters**
 - Click on **Verify Circuit Element Parameters**
 - Click on the Capacitors Tab to verify that there are 91 capacitors
 - Click on the Inductors Tab to verify that there is 25 inductors
 - Click on the Resistors Tab to verify that there are 201 resistors
 - Click OK when finished



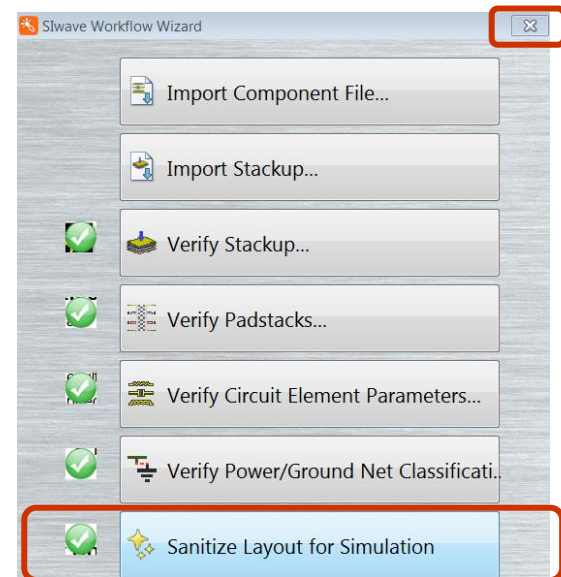
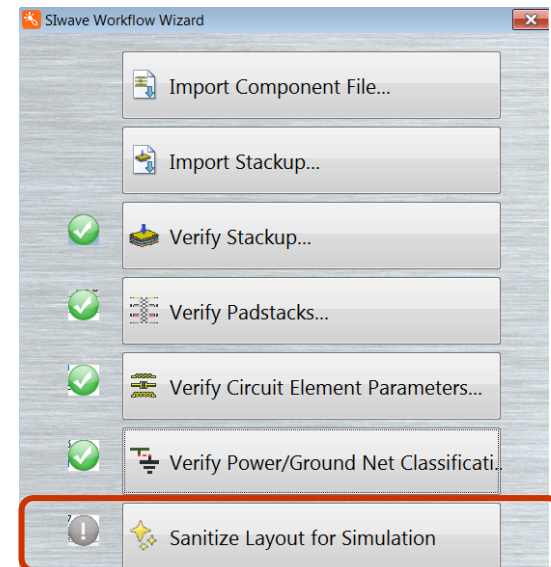
Validation Check

- **Verify Power/Ground Net Classification**

- Click on **Power/Ground Net Classification**
 - Check the classification
 - Click OK when finished



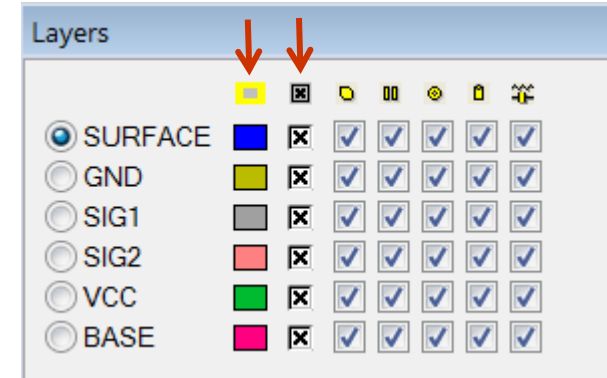
- **Sanitize Layout**
 - Save Validation_check.siw before
 - Click on **Sanitize Layout For Simulation**
- **Notes : It cleans up ECAD Geometry**
 - Results in Higher Simulation Success Rate
 - Speeds up Solver and Reduces RAM usage
 - Heuristically ensures nets identified as PWR/GND have:
 - Planes defined as Planes
 - Traces defined as Traces
 - Overlapping Traces or Traces within Traces are cleaned up
- **Click on the X to close the SIwave Workflow Wizard**



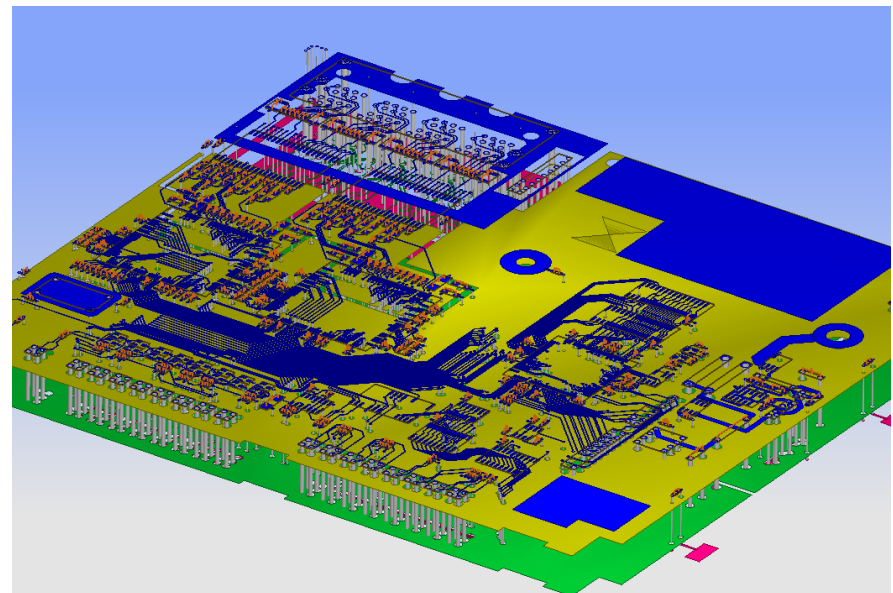
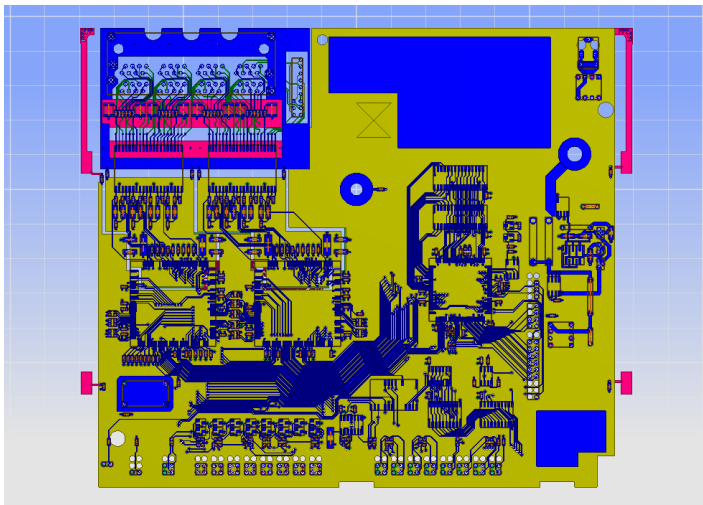
Validation Check

- **Visually inspect the geometry**

- It is important to always look at the PCB structures and ensure they are correct. Some common problems to watch for include: missing planes, mis-aligned edges, and mis-drawn structures.
- Check layers for proper metallization
 - In Workspace Layers :
 - Select the first item to **Fill All** and the second to **Show All layers**

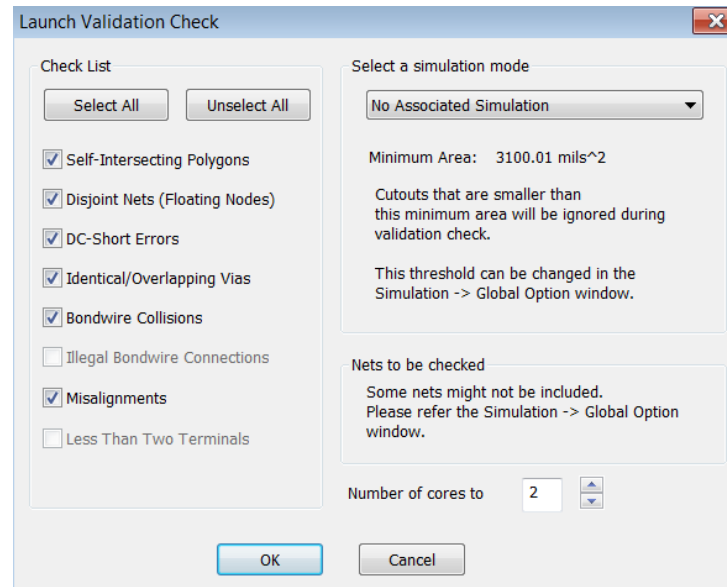
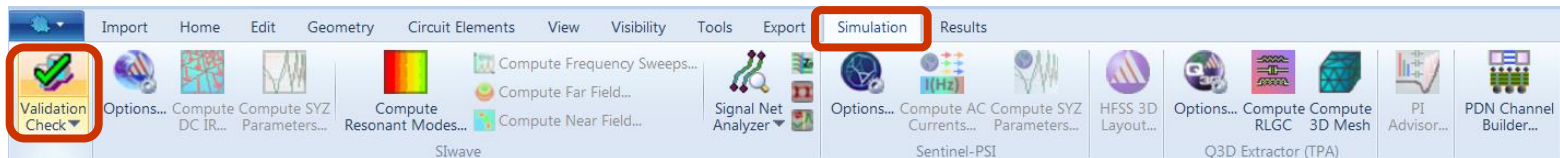


- Verify there are solid planes contained on the PCB
- Verify edges appear to be aligned properly



Validating Imported Design

- SIwave has a very useful automated validation check that will scan your design for potential trouble areas before you even begin to simulate. This checker will flag issues with both layout geometry and electrical violations. If errors are detected they may be corrected in the Layout tool and re-imported, or fixed directly in SIwave.
- The Validation Check tool looks for several different criteria: self-intersecting polygons, disjoint nets, overlapping nets, identical/overlapping vias, collisions of bondwires, illegal connections of bondwires, and trace misalignments.
- To run the validation, go to the **Simulation** tab, select **Validation Check**.
 - Click **OK**.



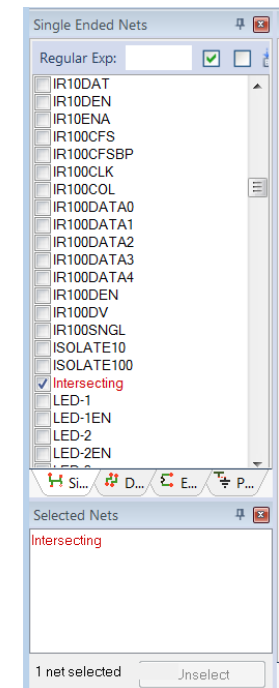
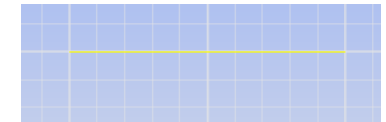
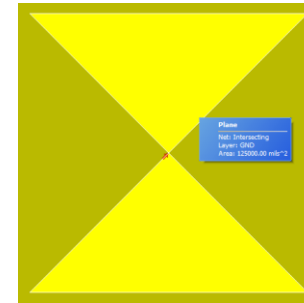
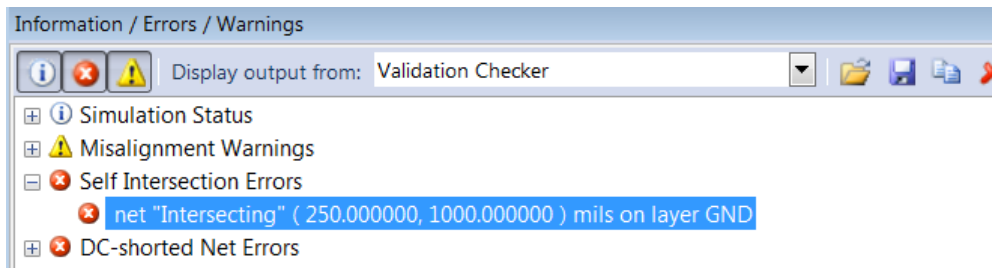
- There should be several errors as shown below. When done reviewing them click OK and the tool will Auto Fix.
- **Notes:**
 - Identical/Overlapping Vias are generally a mistake by the layout engineer accidentally placing two vias instead of one. This is simply corrected by deleting one of the identical vias. SIwave can do this for you automatically.
 - Disjoint Nets highlights trouble with electrical connections. By definition a 'net' is a continuous piece of metal. If two pieces of metal that are defined to be the same net are not touching the net is considered disjoint. A very common problem that arises sometimes is that piece of metal that have been added as shield are not physically connected to ground. These floating pieces of ground can actually serve as a radiating structure rather than provide effective shielding as the engineer was intending. Any floating pieces of metal should be connected through vias/additional metal or removed from layout.

The dialog box titled "Validation Check Results" displays a list of errors and warnings found during a validation check. The "Errors" section lists 16 items, with "Self-Intersecting Polygons" having 1 error and "DC-shortcd Errors" having 16 errors. The "Warnings" section lists 3 items, with "Misalignments (Planes/Traces/Vias)" having 2 warnings. Each item has a count and an "Auto Fix" checkbox. The "OK" button is highlighted in blue.

Category	Item	Count	Auto Fix
Errors	Self-Intersecting Polygons:	1	
	- Circular Loops:	1	<input checked="" type="checkbox"/>
	- Others:	0	
	Point-Connections:	0	
	Disjoint Nets:	0	<input type="checkbox"/>
	DC-shortcd Errors:	16	
	Identical/Overlapping Vias:	0	<input type="checkbox"/>
	Traces-Inside-Traces Errors:	0	<input type="checkbox"/>
	Collisions of Bondwires:	0	
	Illegal Connections of Bondwires:	0	
	Identical Bondwires:	0	<input type="checkbox"/>
Warnings	Misalignments (Planes/Traces/Vias):	2	<input checked="" type="checkbox"/>
	Bondwires Misaligned With Die Pads:	0	<input type="checkbox"/>
	Pins Shared By Multiple Pin Groups:	0	<input type="checkbox"/>
	Reversed Bondwires:	0	<input type="checkbox"/>
	Floating Nodes:	0	<input type="checkbox"/>
Zero Via Plating:	0		
Nets With Less Than 2 Terminals:	0		

• Notes (Continued)

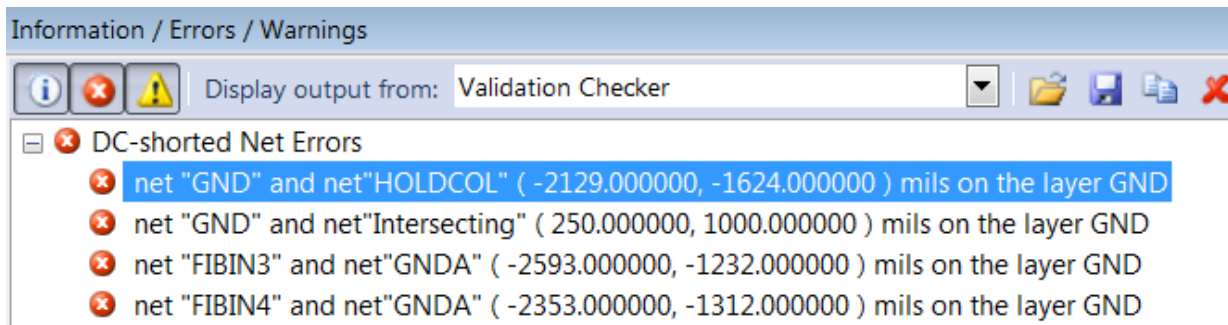
- Self-intersecting polygons are generally a problem with layout. Often these can be flagged and fixed using a DRC in the original layout tool. The problem generally arises from a polygon that has improperly defined points. Sometimes due to a precision error or user error a polygon may double back on itself and create a region that cannot be filled. Another common self-intersection error is when two sections of a polygon meet at specific point. This point can cause trouble in manufacturing and in simulation because it is an section with zero area associated with the polygon.
- To see and correct the issues:
 - Expand the error message window at the bottom of the screen



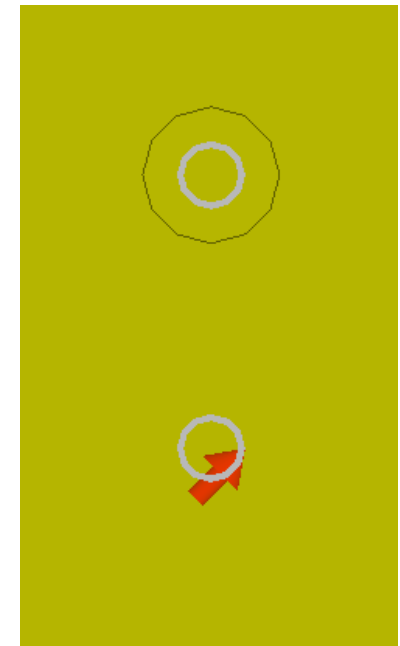
- Click on the coordinates listed by the error – SIwave will zoom to the location.
- Zoom out slightly so you can see the entire shape.
- Self-intersections can be corrected by modifying the geometry, this typically includes:
 - Drawing/merging over errant point
 - Deleting errant geometry
 - Editing points of polygon
- Since this geometry fully contained within the ground plane
- and not relevant electrically we can safely delete it.
- Select “Intersecting” net in the netlist
 - Press the Delete key

- **Notes (Continued)**

- Overlapping Nets are when two separate nets make a DC connection. This can occur when geometry is misdrawn, vias do not have antipads or when dielectric layers have 0 thickness. These problems should be viewed and corrected on a case by case bases.
- To see the DC Short problems:
 - Expand the DC shorts message window

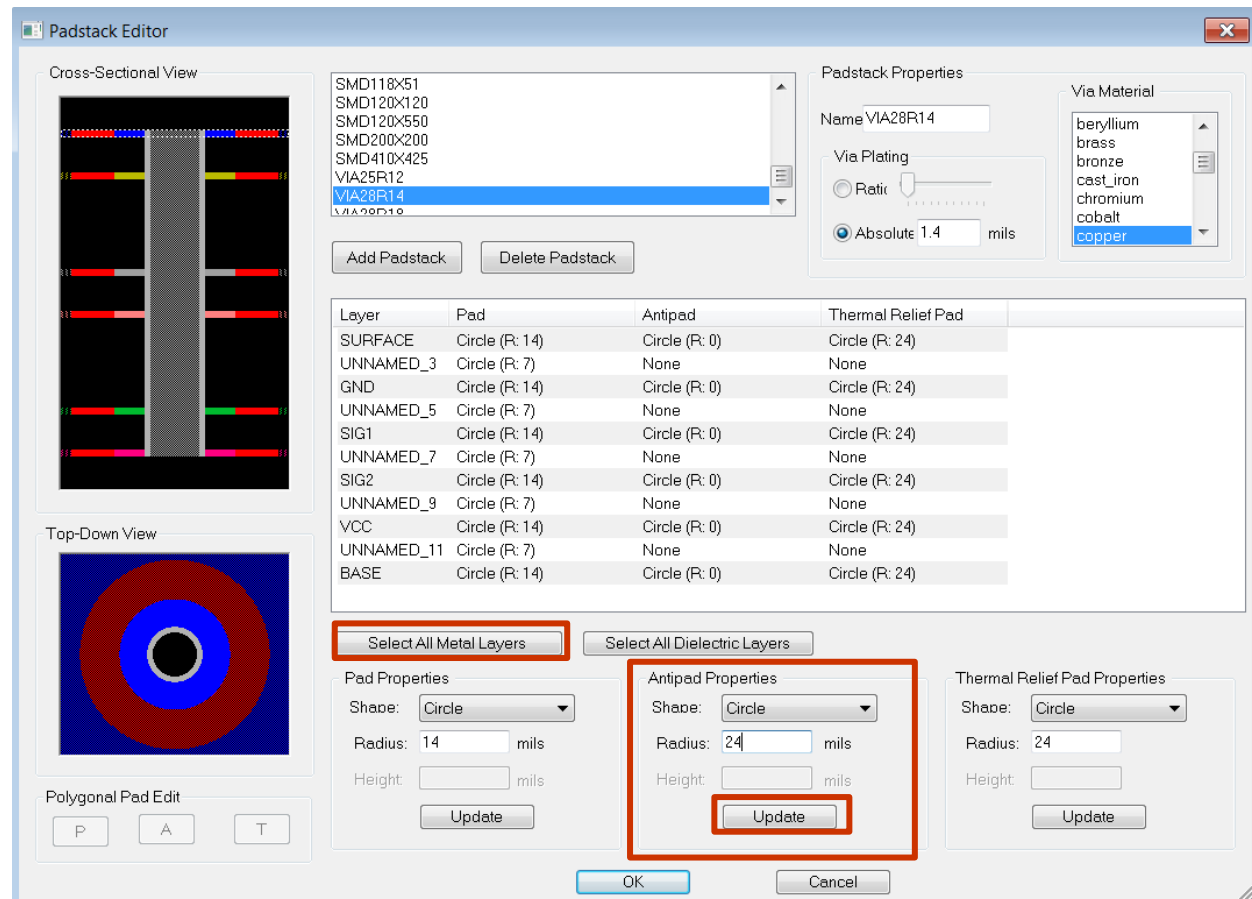
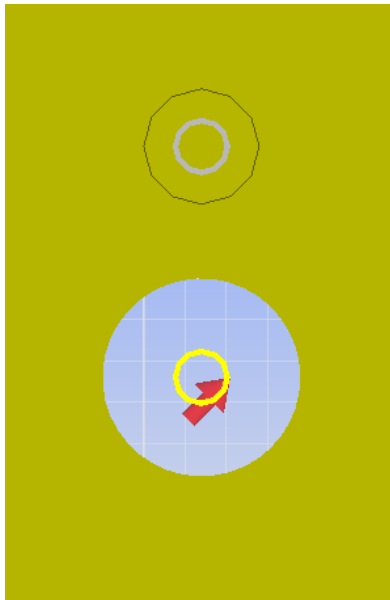


- Click on the coordinates of the first error to visualize the problem



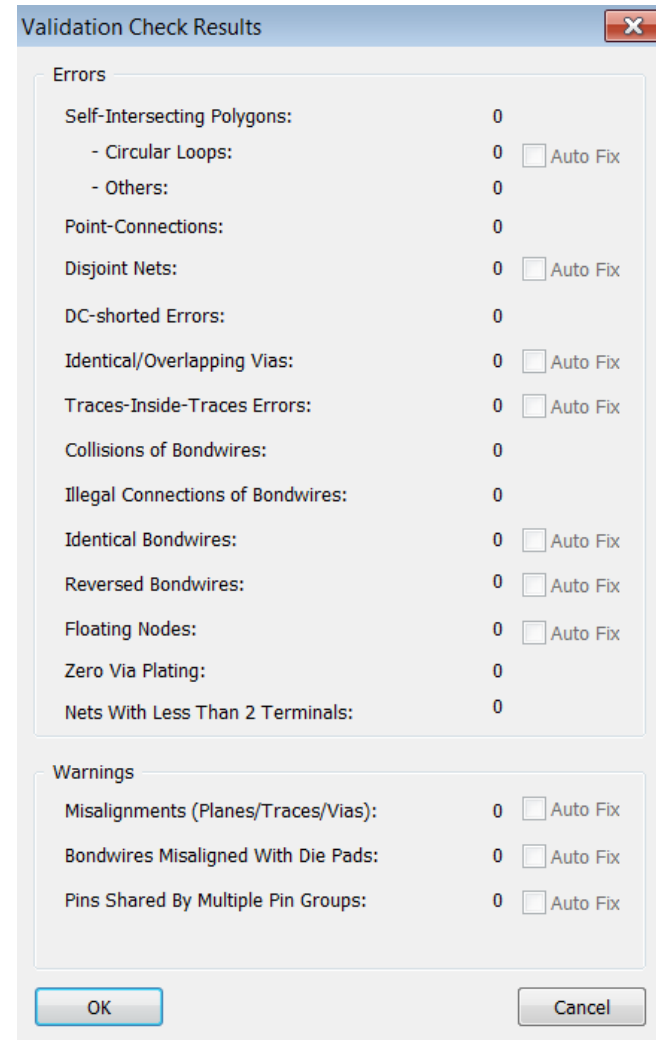
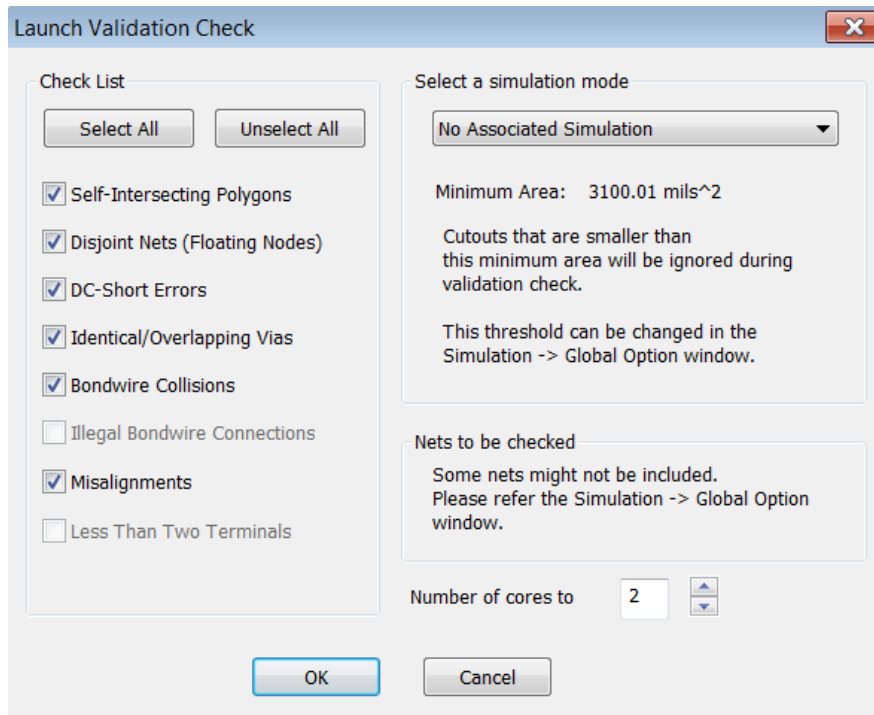
Validation Check

- In this case it looks like the antipad was not defined for this particular padstack.
- Select the via pointed to by the red arrow by clicking on it
- Click **Home > Edit Padstacks** to modify the padstack
- Hold down the **Ctrl** key and select all of the metal layers or click the **Select All Metal Layers** button.
- From the Shape pull down menu under *Antipad Properties* select **Circle**
- Enter Radius: **24 mils**
- Click **Update**
- Click **OK**



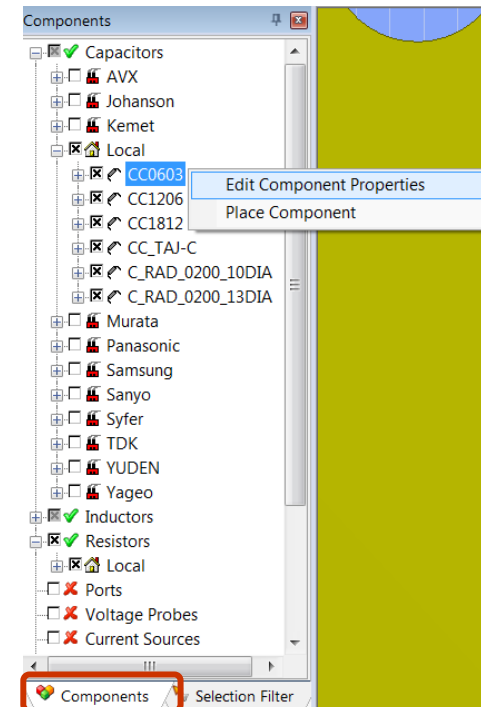
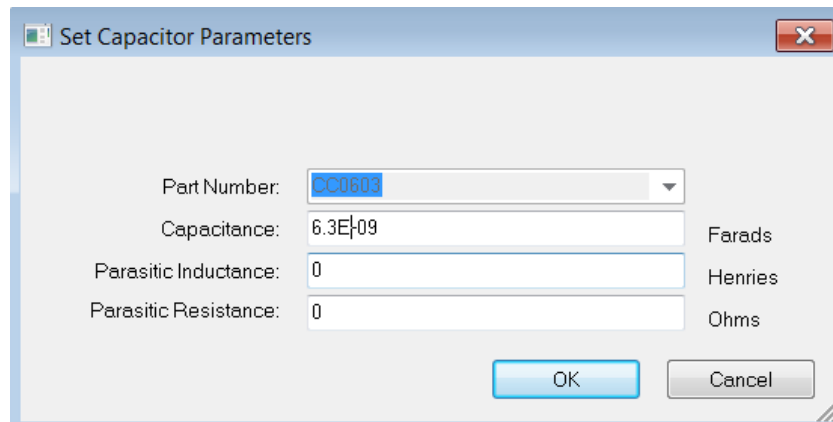
Validation Check

- Since the padstack we edited may be used by many vias, rerun the validation check to see if any errors remain
 - Select the menu item **Tools > Validation Check...**
 - Click **OK** to run the validation check
 - Verify all tests return 0 errors
 - Click **OK** to exit

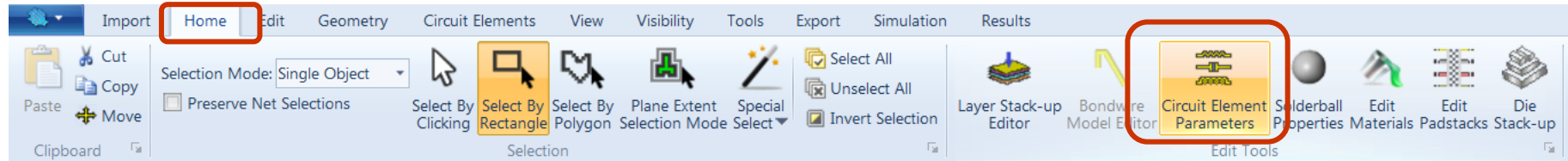


• Examine Components

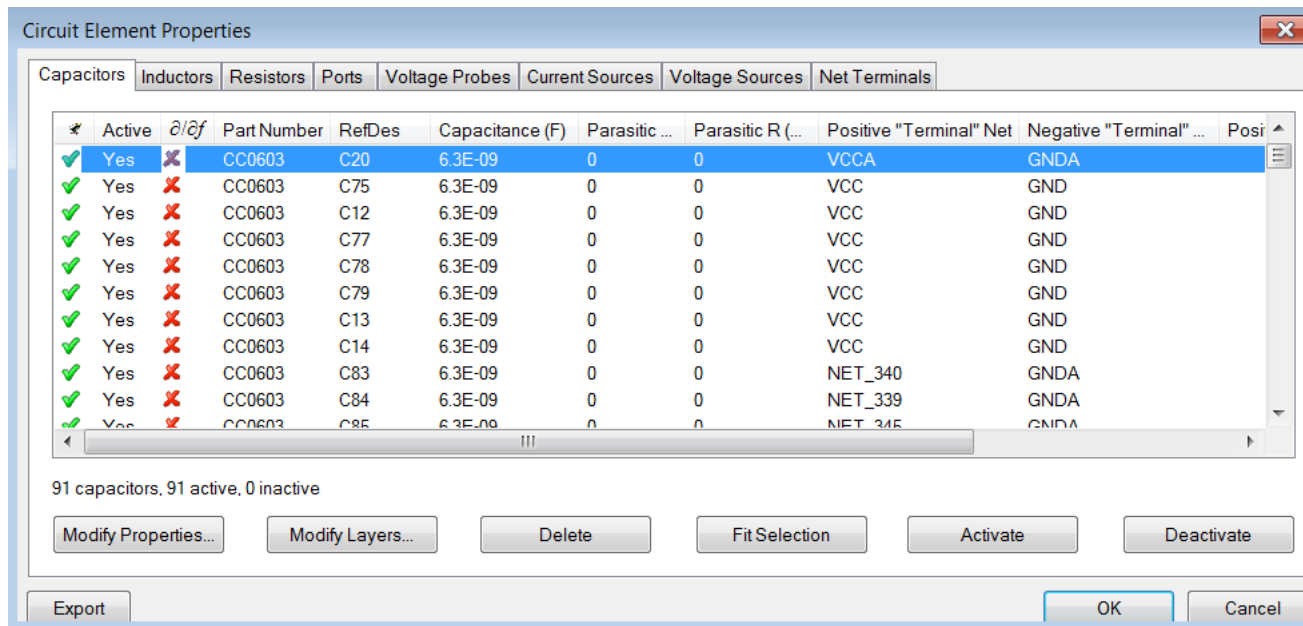
- Components are another item that are very important for electrical simulation. All of the values, names, and reference designators will be imported from the layout tool, however it is essential the simulation engineer verifies the correctness of the components.
- Verify the component values
 - From the **Home** tab, click on **Circuit Element Parameters** button
 - Inspect the values of the capacitors by scrolling through the list
 - Notice all of the values are $1\text{e-}7$ which is the default value when none is available from the layout software
 - Click **OK**
 - Click on the **Components** tab in the sidebar, if the components tab is not present make sure that the following is checked: **View > Workspaces > Components**.
 - Expand the **Capacitors** listing
 - Expand the **Local** listing
 - Right click **CC0603** and choose Edit Component Properties
 - Change the capacitance to **$6.3\text{e-}9$**
 - Click **OK**



Validation Check



- From the **Home** tab, click on **Circuit Element Parameters** button
- Verify the values for the CC0603 capacitors have been updated



- In a real design this same procedure should be followed for the remaining capacitors, inductors, and resistors with the values from the bill of materials for the design