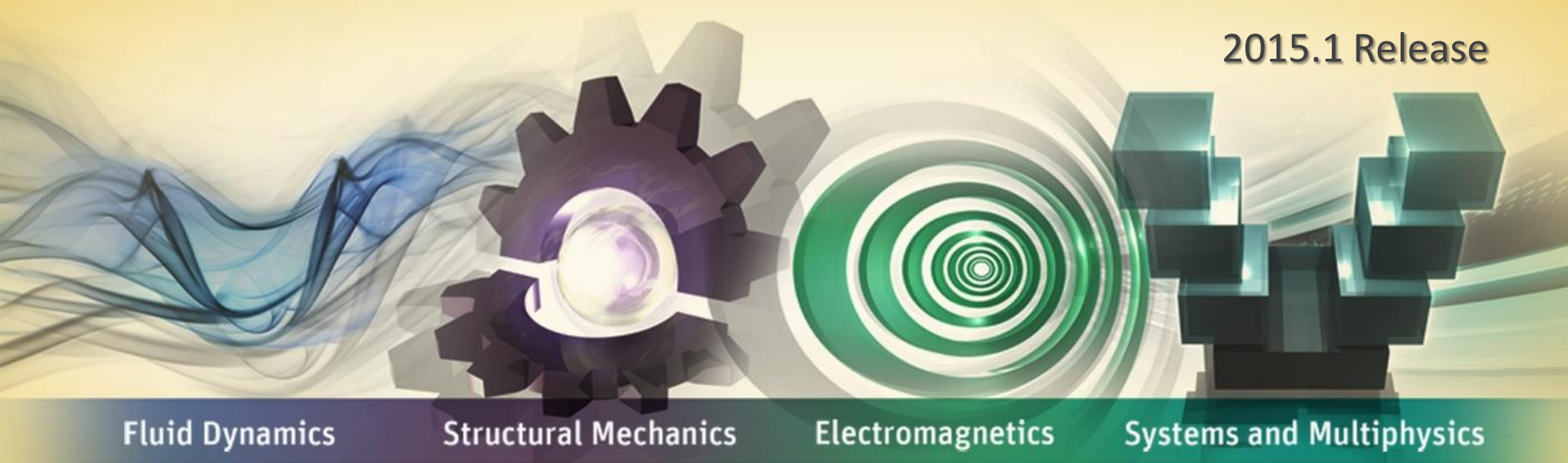


Workshop 8: DCIR

2015.1 Release



Fluid Dynamics

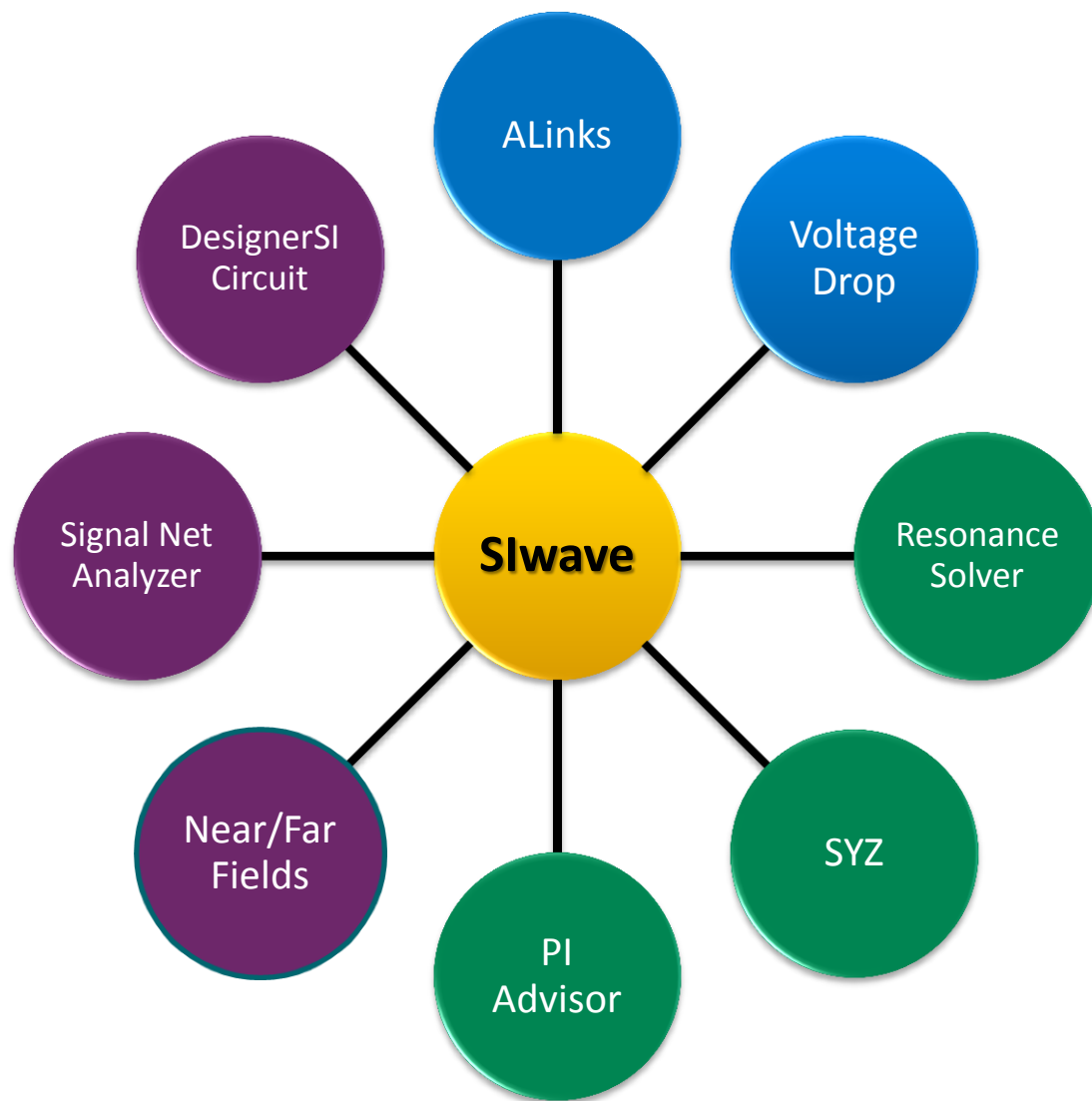
Structural Mechanics

Electromagnetics

Systems and Multiphysics

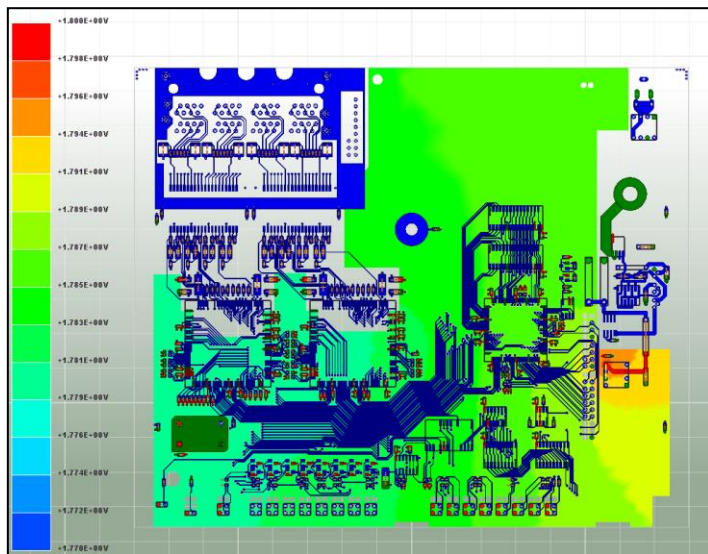
Introduction to ANSYS SIwave

ANSYS SIwave 2015 – 3 Levels

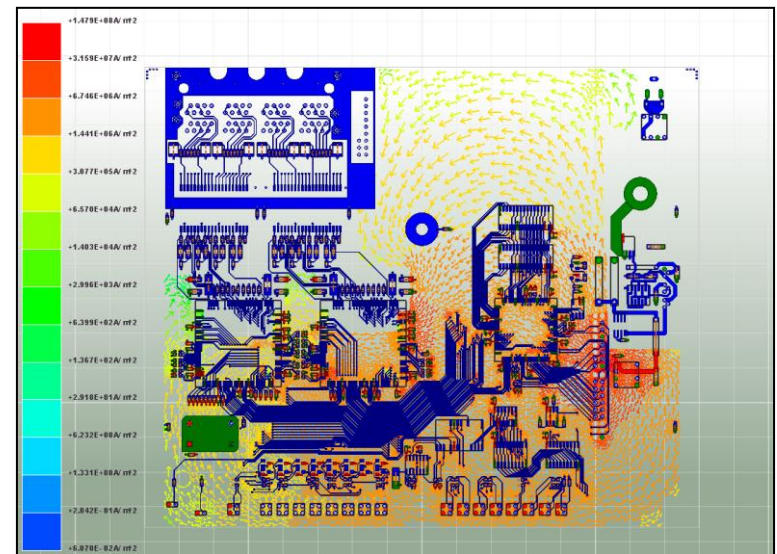


Release scheduled in Q1 2015

- **SIwave DC** – includes all the essentials to import a design and setup DC simulations for packages and PCBs and the combination of the two. This includes:
 - DC voltage drop (Voltage) for all nets including Traces, Ground and Power
 - DC current direction (Amps/Area2) that includes return paths
 - DC current magnitude (Amps) into and out of vias
 - Power density (W/Area2) and power loss (Watts) per layer
 - Bi-directional coupling to Icepak for thermal loss simulations (joule heating)
 - Automated report generation with user defined pass/fail criteria



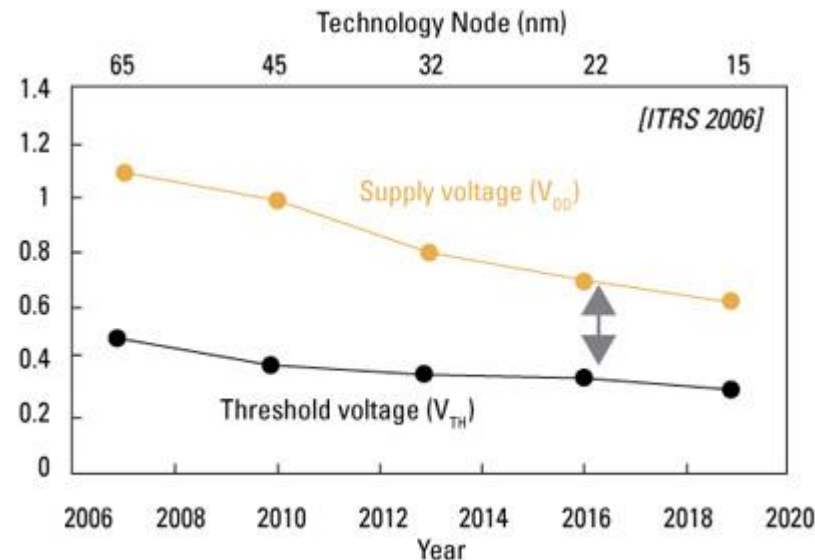
Voltage Drop



Current Density

Why is it important to run DC IR simulations?

- Supplying clean and sufficient power to today's high speed semiconductors is a major bottleneck in the industry
- With the trend of adding more functionality into every integrated circuit, the design challenges of being able to operate many different IC functions into an ever shrinking area has proven to be one of the biggest challenges to Power Integrity engineers
- Being able to simulate these power rails has become critical to design systems that:
 - Avoid DC current crowding in planes, traces and vias which can lead to PCB failures and bad circuit performance
 - Debug existing PCB designs to make minor layout changes that result in major performance and reliability improvements
 - Reduce design spins
 - Decrease warranty costs associated with thermal-cycling issues



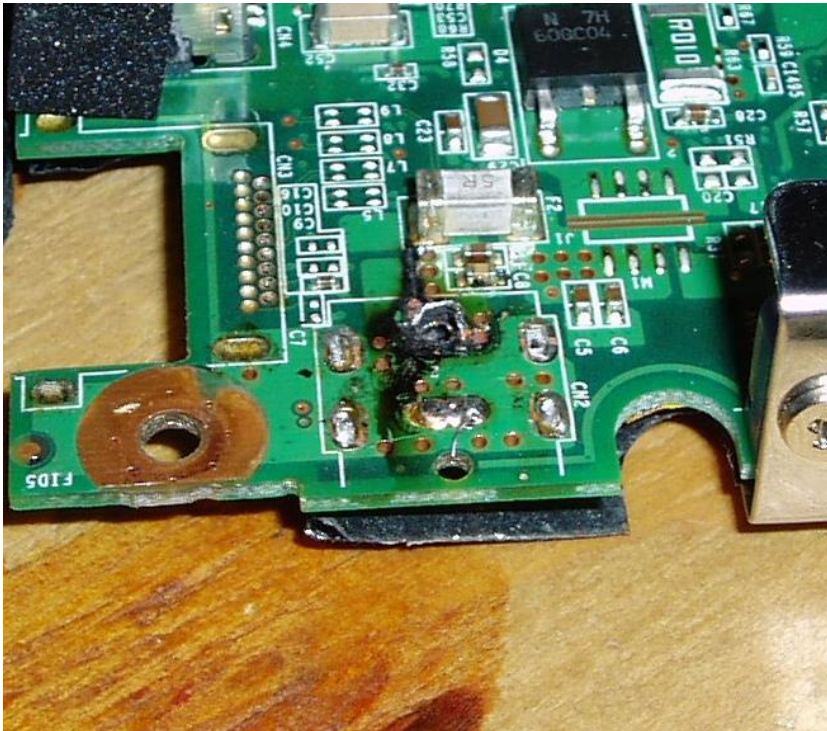
The importance of DC simulations

- **Failures**

- Lack of good DC design may not lead to high DC resistance but it can cause “thermal hot spots” due to the excessive heating and product failures

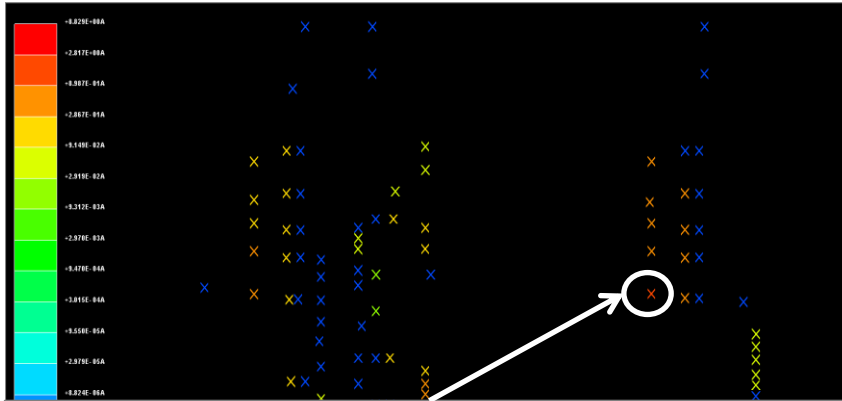
- **Solution**

- Robust and accurate DC and PDN design results in a more even spread of the current density and reduces risk of failure.

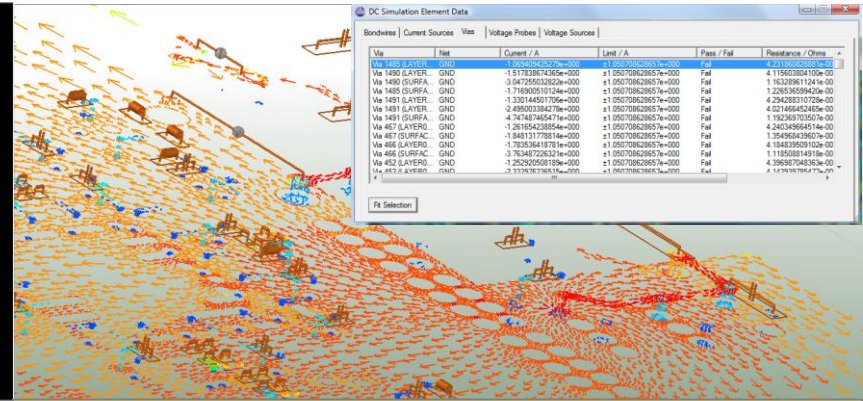


- A new product offering specialized for predicting DC power delivery issues within PKGs and PCBs
- The solver uses a unique **Adaptive Mesh Refinement** process to ensure highly accurate predictive analyses for **Chip, Packages, and Printed Circuit Boards** which include ECAD primitives such as planes, traces, vias, bondwires, solderballs and solderbumps
- **Produces the following analytic results**
 - DC voltage drop (Voltage) for all nets including GND and V_{dd}
 - DC current direction (Amps/Area²) that includes return paths
 - DC current magnitude (Amps) into and out of vias
 - Power density (W/Area²) and power loss (Watts) per layer
 - Verification of via and bondwire DC tolerances
 - Calculation of path resistances between sources and sinks
- **Partial resistance computation between any two user-defined locations in layout**
- **Has bi-directional coupling to Icepak to account for thermal losses (joule heating)**
- **Automated reports for user defined pass/fail criteria using .html formats**

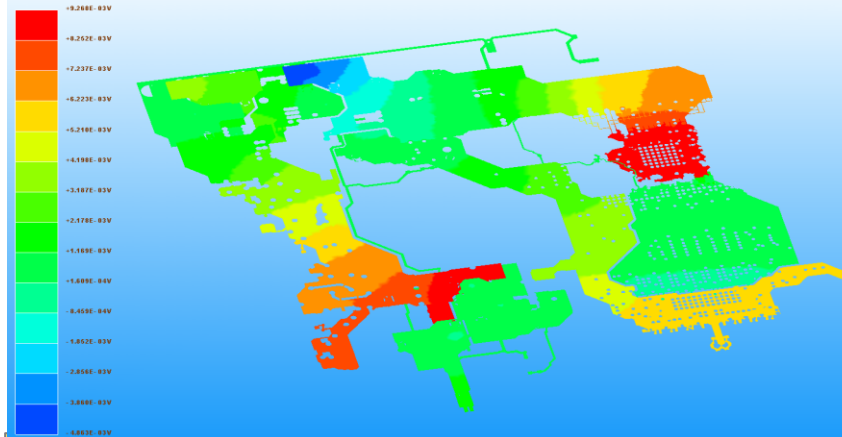
SIwave DC Results & Analysis



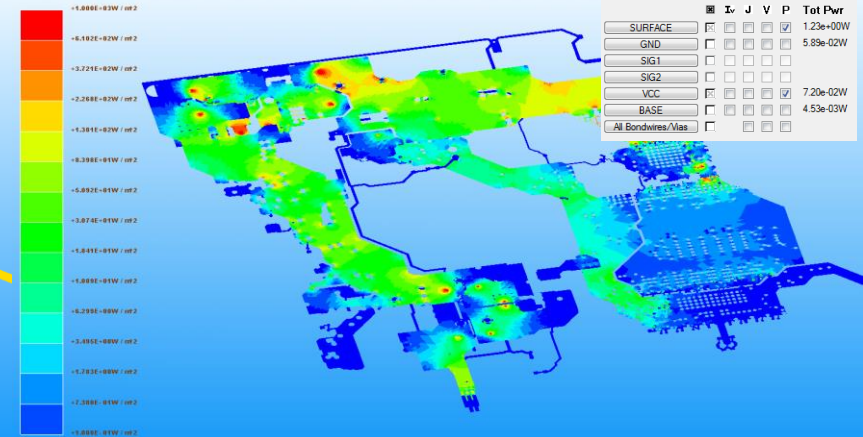
Via Current Hot Spot Detection with Direction



Current Vectors Showing Electron Direction

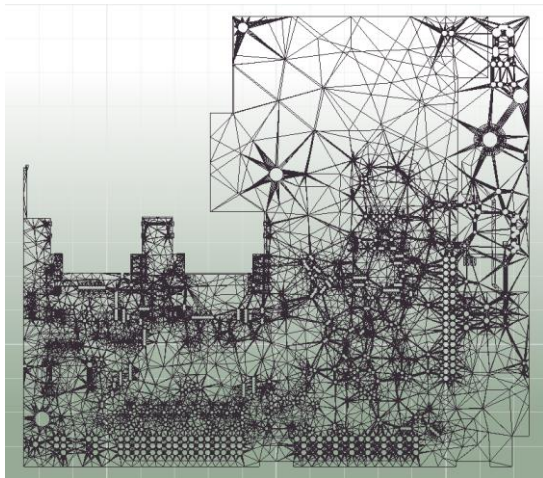


Voltage Drop across Vcc

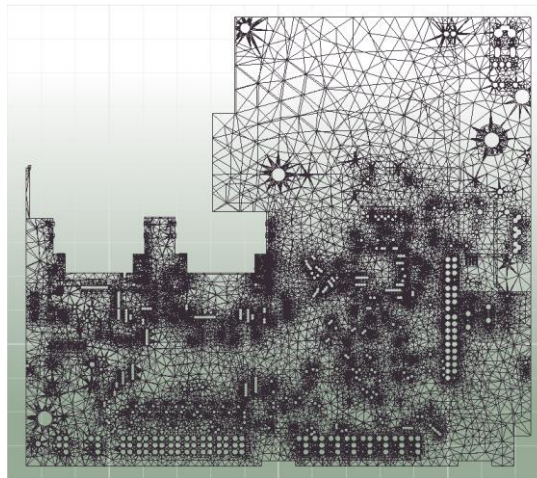


Power Loss Across Vcc

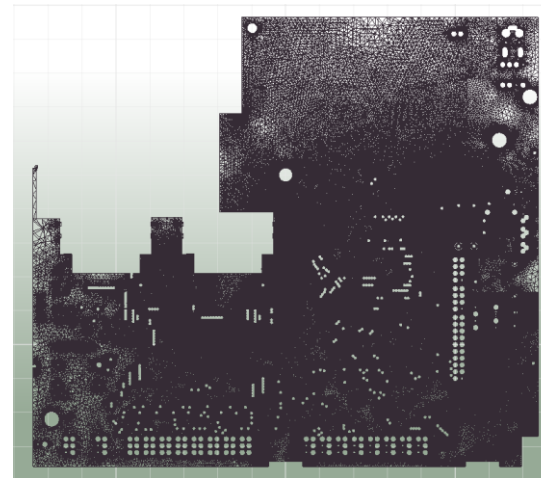
- **DC Adaptive Mesh Refinement**
 - Ensures accuracy by refining the mesh



1 Adaptive Pass



3 Adaptive Pass



20 Adaptive Pass

SIwave – DC Current and Voltage Analysis

- **DC Current and Voltage Analysis**

- This training examples steps the user through the methodology to setup and solve a DC current and voltage analysis. It allows the user to define the power rail(s) of interest as well as the current loads and voltage being supplied. The results from the simulation allow the user to visually see the voltage drop across the power net, visually see the current flow, obtain tabular data for the current and resistance for the vias, and obtain loop resistance values from the VRM to the IC.
- The goal of the DC Current and Voltage Analysis is to get accurate current, resistance, and voltage values to determine the performance of the power rails.

Example – DC Current and Voltage Analysis

- **ANSYS Siwave Design Environment**

- The following features of the ANSYS Siwave Design Environment are used to simulate the Current and Voltage Analysis.
 - Verification of board import
 - Check stack up
 - Check nets
 - Check discrete components (Capacitors, Resistors, Inductors)
 - Generate pin groups
 - Create pin groups on power rail
 - Create pin groups on ground net
 - Create Sources
 - Add Voltage source
 - Add Current source
 - Solution Setup and Solve
 - Run a simulation to Compute DC Current/Voltage
 - Plotting and analyzing results
 - Visually inspect the current flow
 - Visually inspect voltage along power rail
 - View tabular data for current and resistance for vias
 - View loop resistance from VRM to current loads

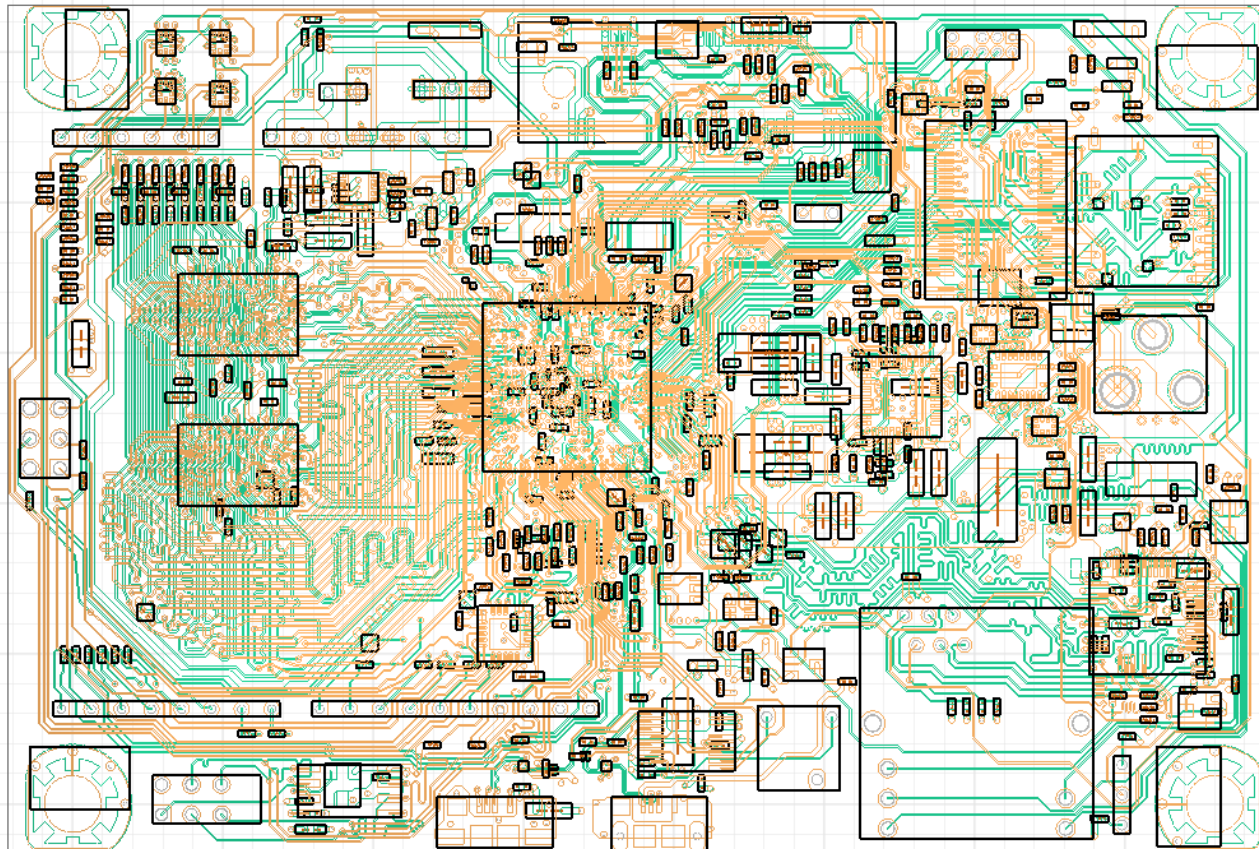
Example – DC Current and Voltage Analysis

- **Starting Slwave**

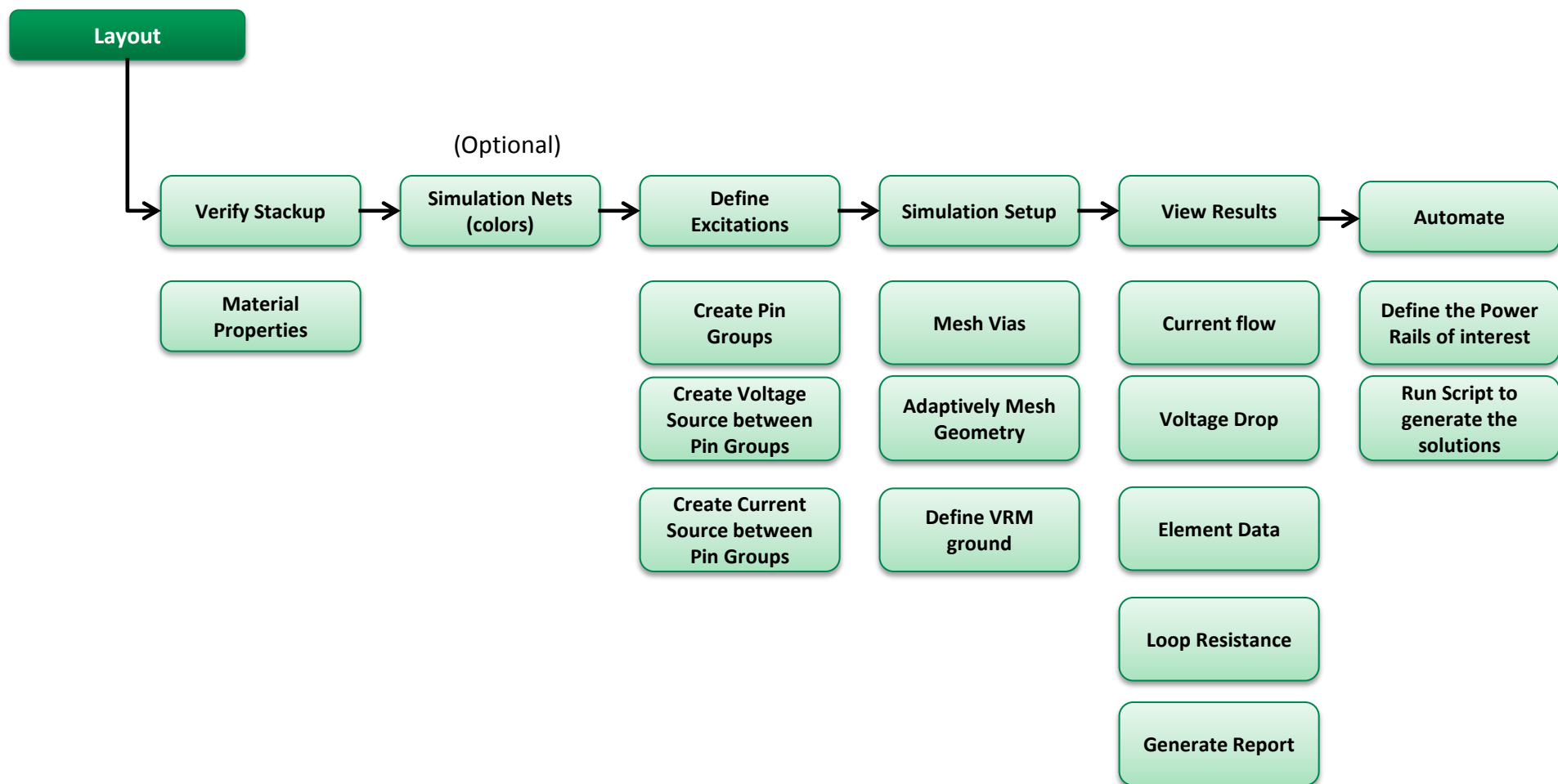
- To launch Slwave program, click the Microsoft **Start** Button, select **Programs**, select **ANSYS Electromagnetics** program group
- Select the **ANSYS Electromagnetics Suite 16.1 > ANSYS Slwave2015.1**

- **Open a Slwave Project**

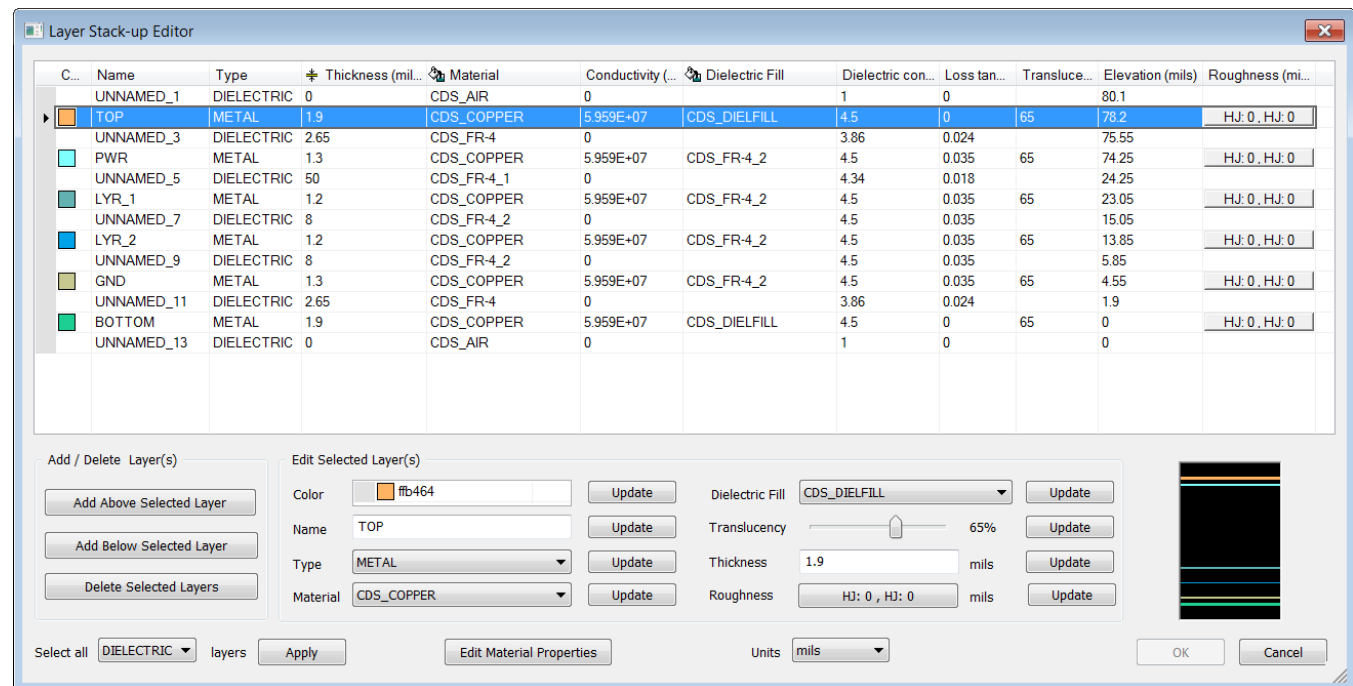
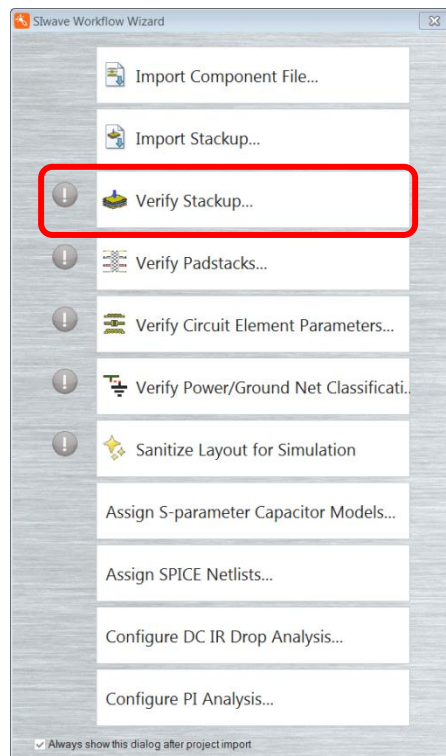
- Select the menu item **File > Open**
 - Browse for file: **DCIR.siw**
 - Click the **Open** button



SIwave – DC Current and Voltage Analysis Design Setup

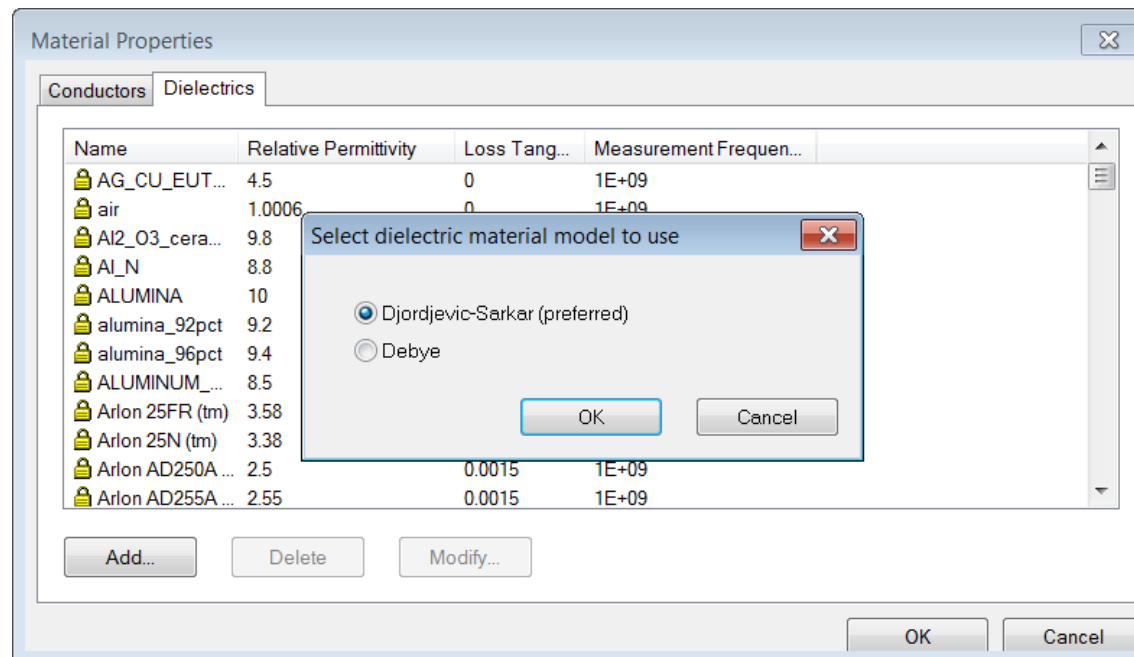
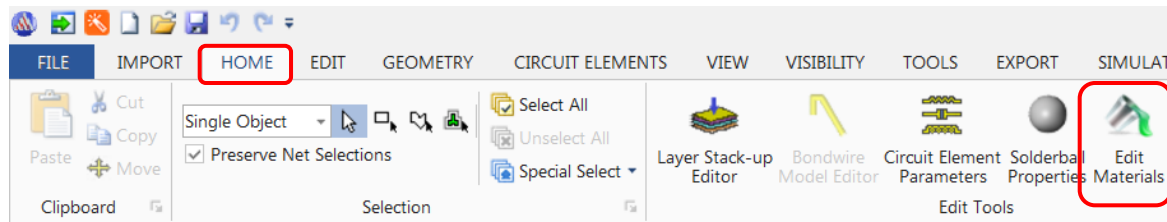


- **The SIwave Workflow Wizard walks through the steps to make a project simulation ready**
 - Since an existing project was opened, the first two steps, Import Component File and Import Stackup can be skipped. The first step in this example will be to Verify Stackup
 - Click Verify Stackup to bring up the Layer Stack-up Editor
 - Verify the Stackup and Material Properties and Click OK when finished

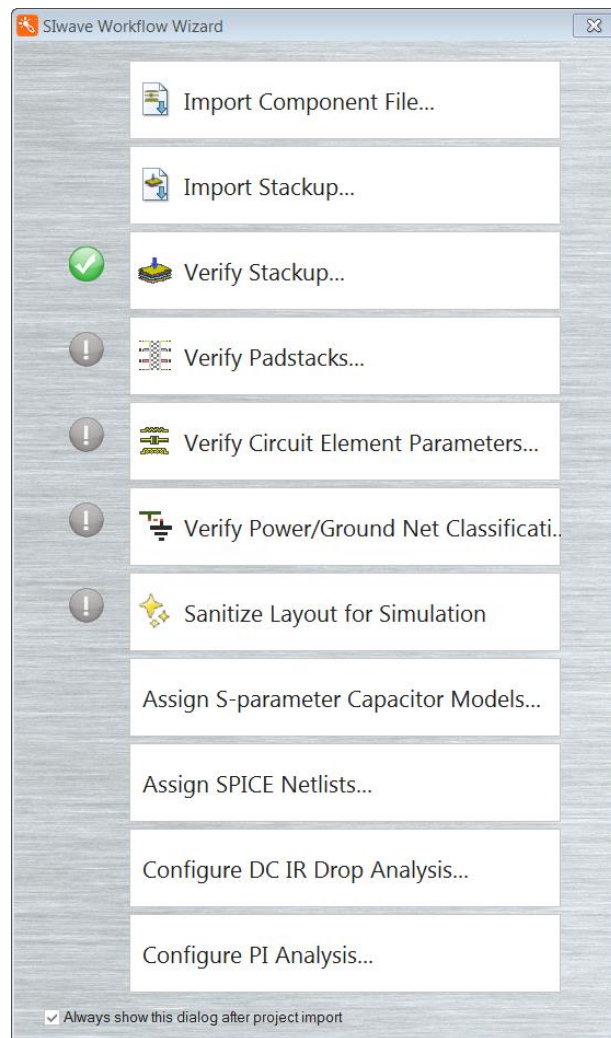


- **Adding Materials**

- To add dielectric material select **Home > Edit Materials > Dielectrics**. Click on **Add** and type in known values for your dielectric
 - Layers with constant material permittivity greater than one and dielectric loss tangent greater than zero will be treated as frequency dependent. Their actual permittivity and conductivity will be determined by the Djordjevic-Sarkar algorithm.



- The Verify Stackup will now be checked in the SIwave Workflow Wizard



View Layers and Change Nets Colors

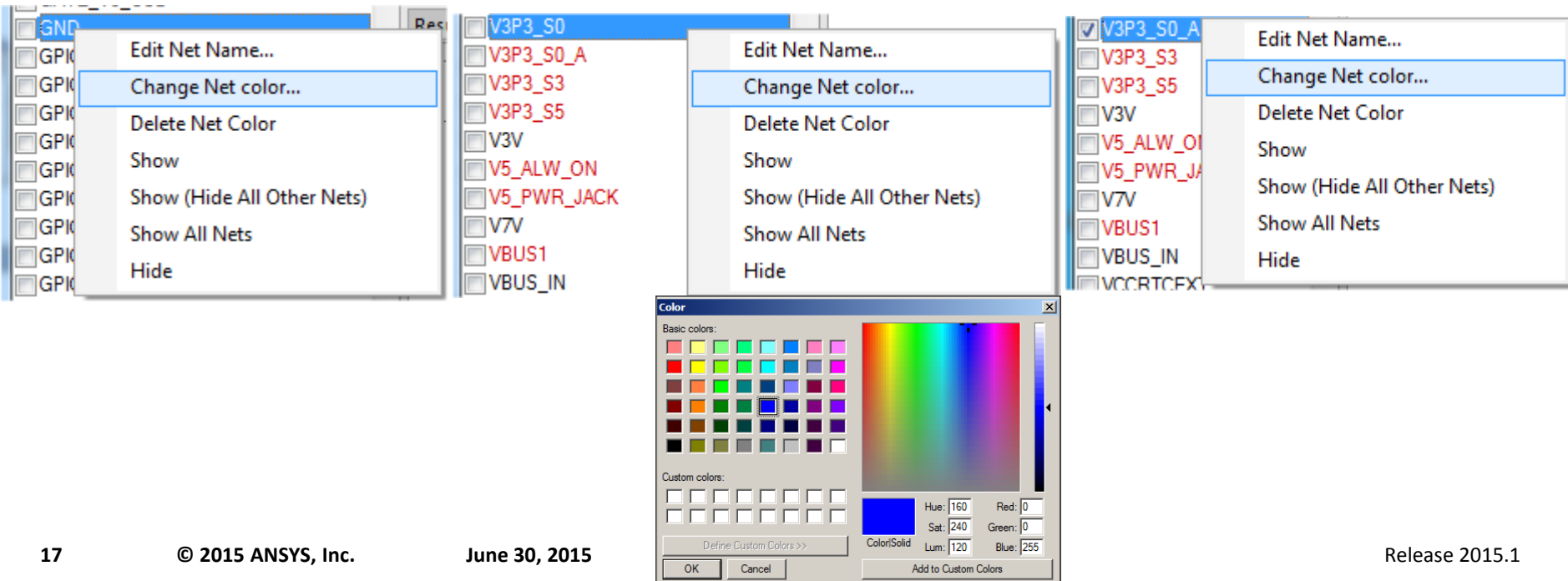
Change Nets
Colors

(Optional)

View Layers and Change Nets Colors

• Change Net Colors

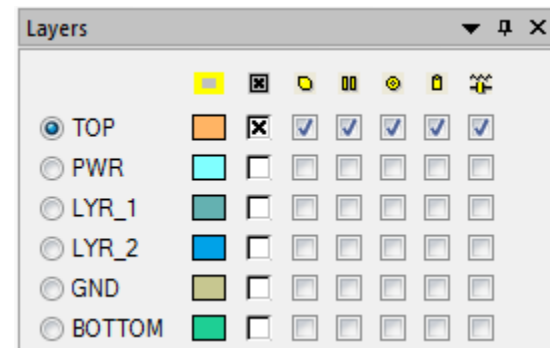
- For easier visualization of complex PCB layouts it is recommended to change net colors.
- To change net color click on one nets of your choice and
 - Right mouse click GND
 - Click **Change Net Color...**
 - Select **Green** in the color palate
 - Click OK to exit
- Select and change colors for the following two nets:
 - **V3P3_S0** -> New Net Color: **RED**
 - **V3P3_S0_A** -> New Net Color: **BLUE**



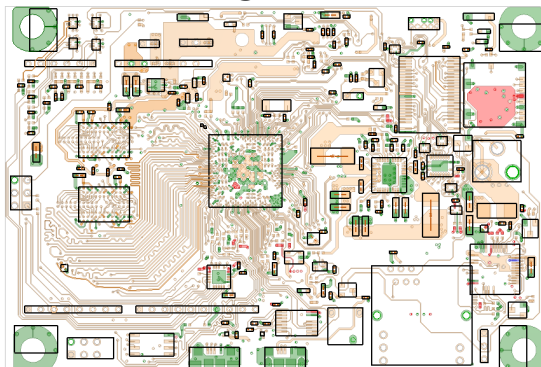
View Layers

• View Layers

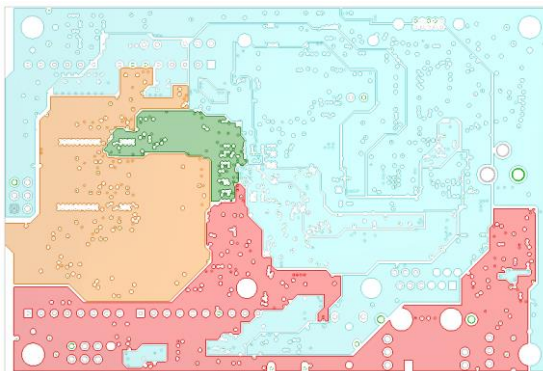
- To view each layer separately enable or disable the visibility for each layer in the Layers sub window



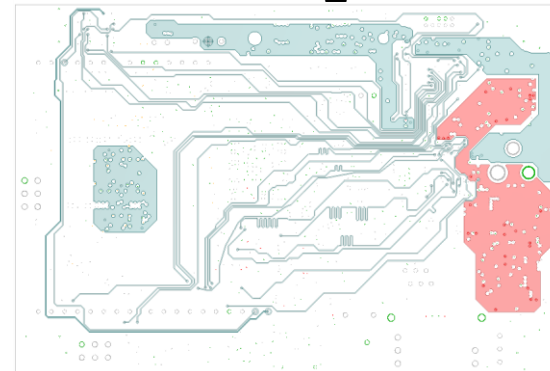
TOP



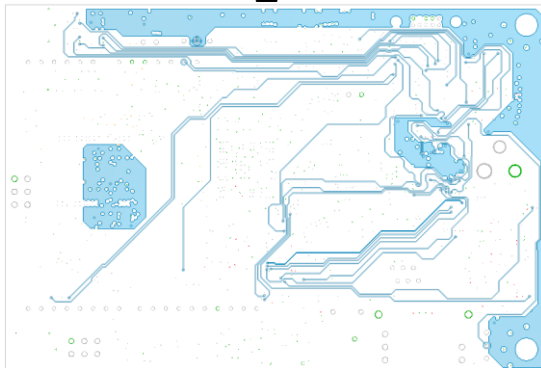
PWR



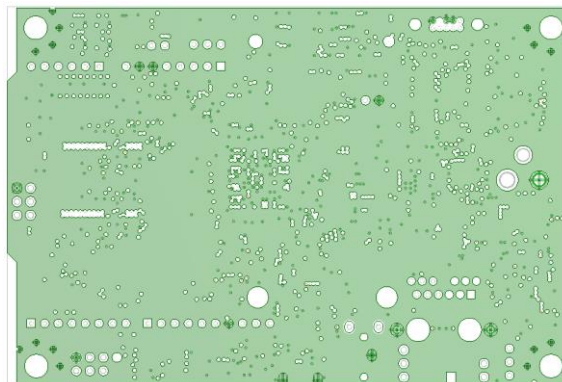
LYR_1



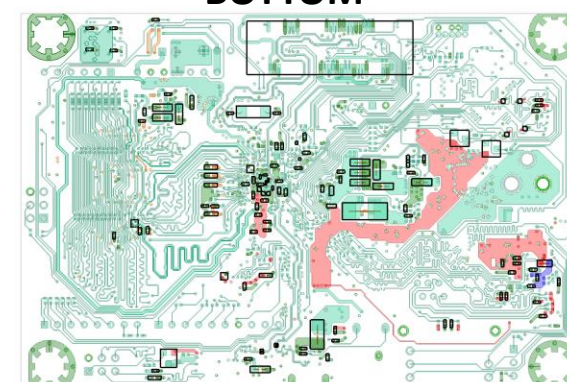
LYR_2



GND



BOTTOM

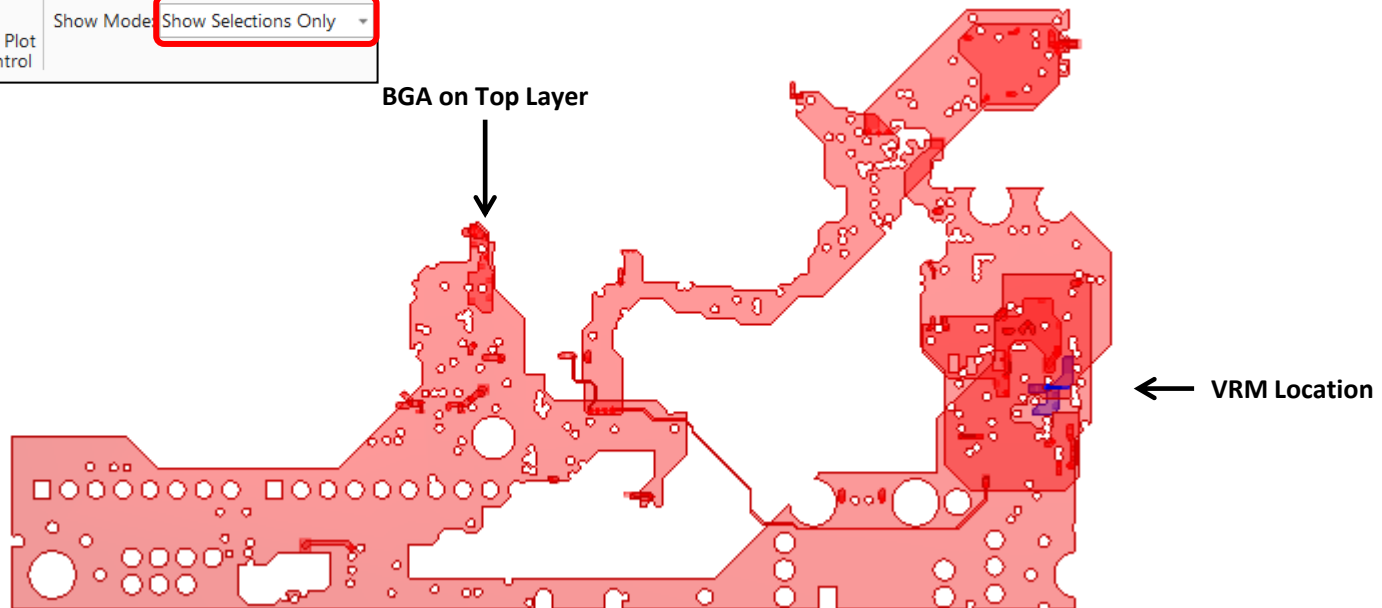
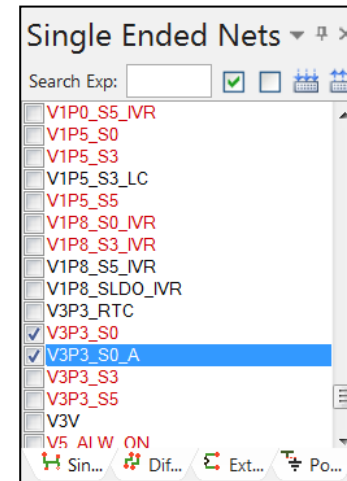
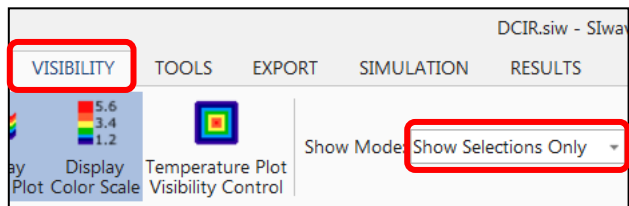


- **To view the power rail only**

- Place check marks in the Selected Nets workspace for:

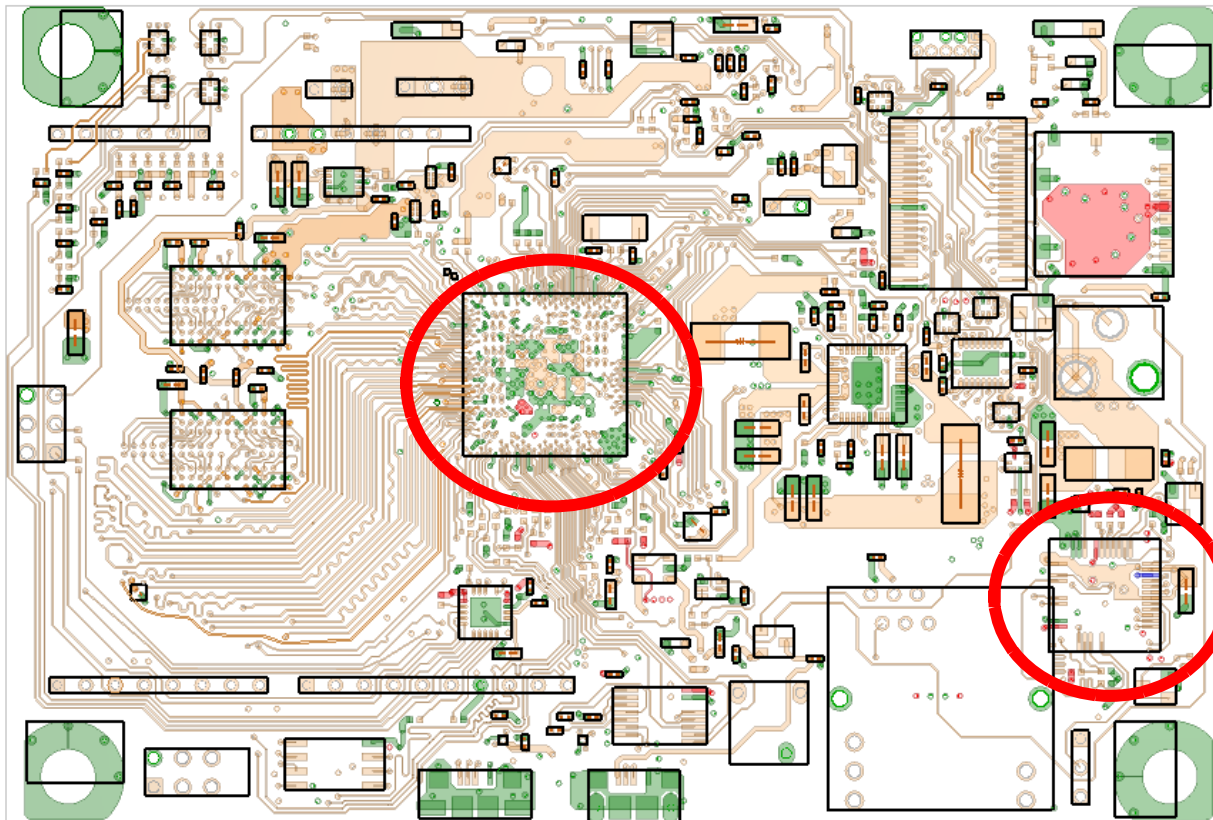
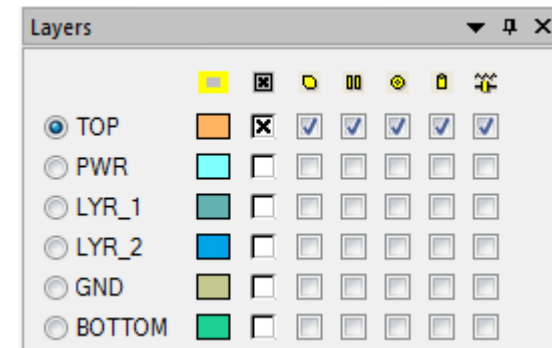
- V3P3_S0
- V3P3_S0_A

- Click Visibility > Show Mode: Show Selections Only



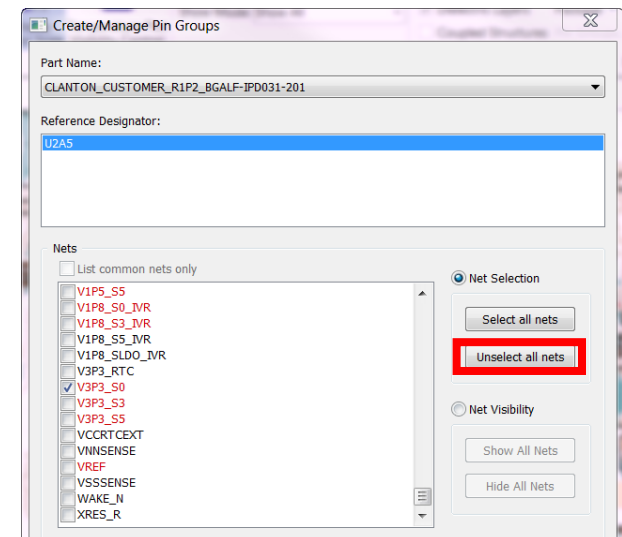
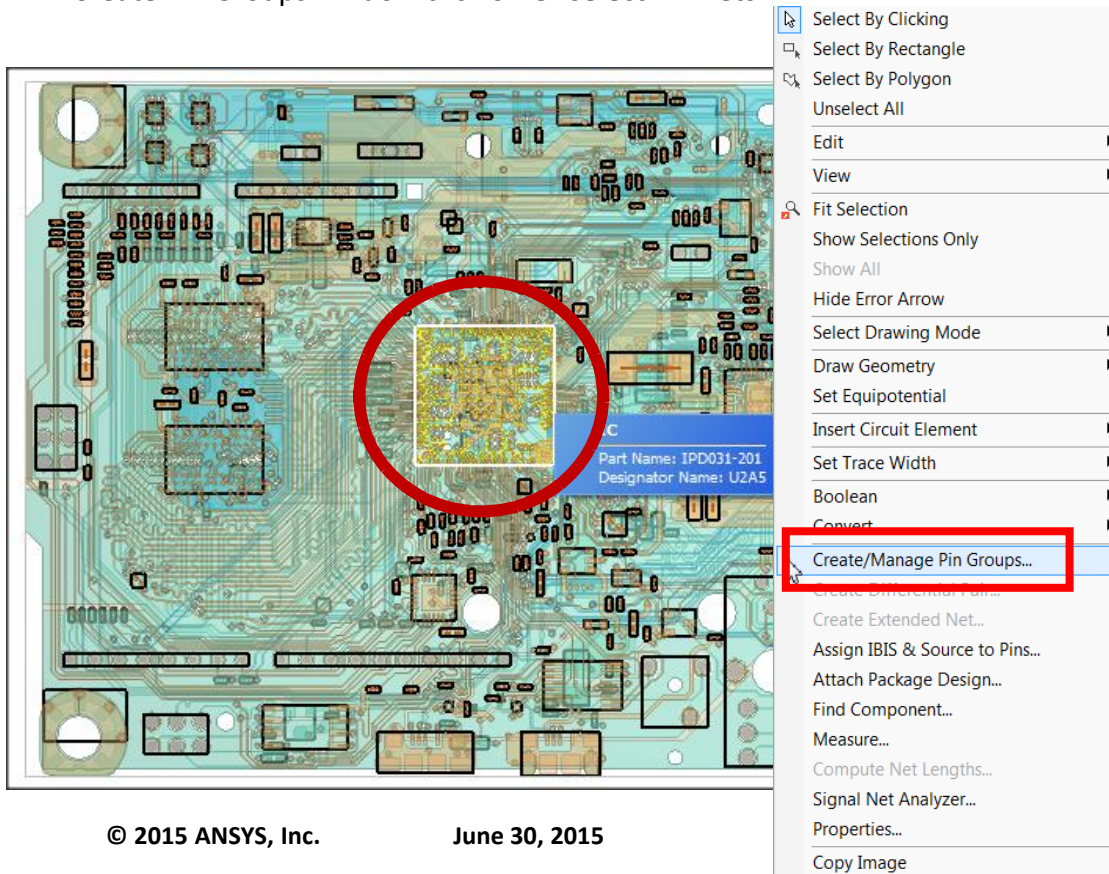
View TOP Layer

- Enable the visibility for TOP layer only
- Click **Visibility > Show Mode > Show All**
- **Encircled below are two components that will be used in simulations**
 - Pin groups will be created on these two components



Excitations (Pin Grouping)

- For DC Current and Voltage simulations, voltage and current sources must be added at the components of interest.
 - We will define these sources between power and ground groups of pins on BGA U2A5 and U4B1 components.
- In SIwave UI click and highlight the outline of BGA (U2A5) component
 - When selected, right mouse click and choose **Create/Manage Pin Groups...**
 - In Create Pin Groups window click on **Unselect All Nets**



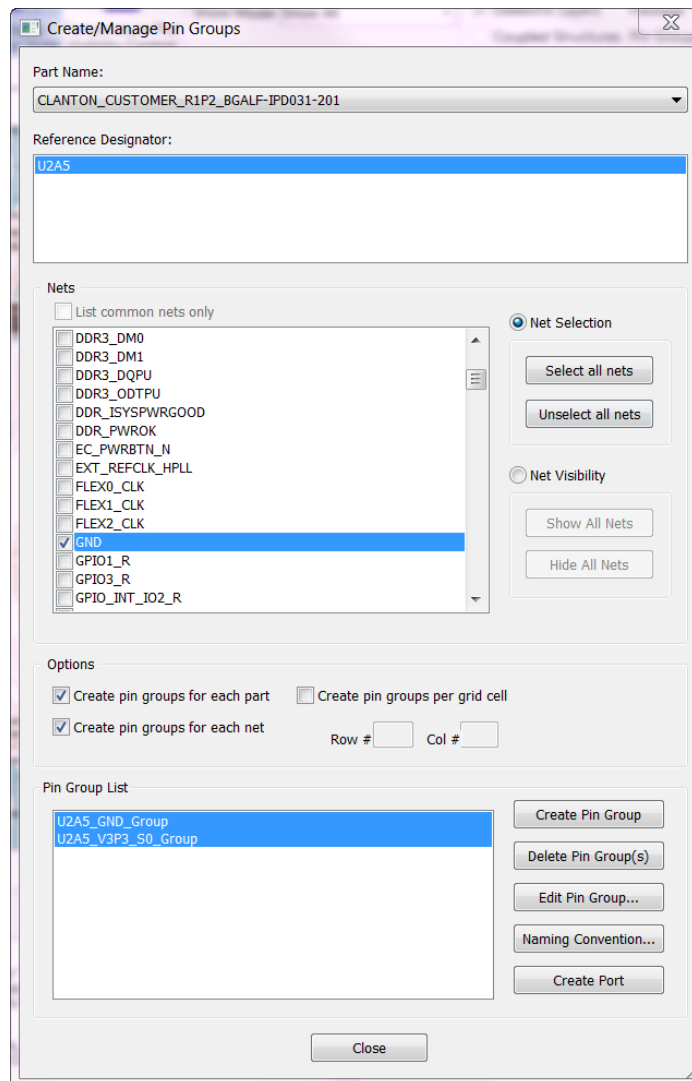
Excitations (Pin Grouping)

- In SIwave UI click and highlight the outline of BGA (U2A5) component

- In the Net List select **GND** and **V3P3_SO** nets
- Check **Create pin groups for each part**
- Check **Create pin groups for each net**
- Click the **Create Pin Group** button

- Repeat for the U4B1 component

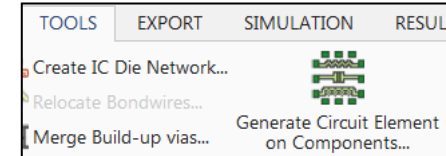
- Select Part Name **DP83848I_LQFPLF-G60296-001**
- Select **GND** and **V3P3_SO_A** nets
- Check **Create pin groups for each part**
- Check **Create pin groups for each net**
- Click the **Create Pin Group** button
- Click **Close**



Excitations (Ports)

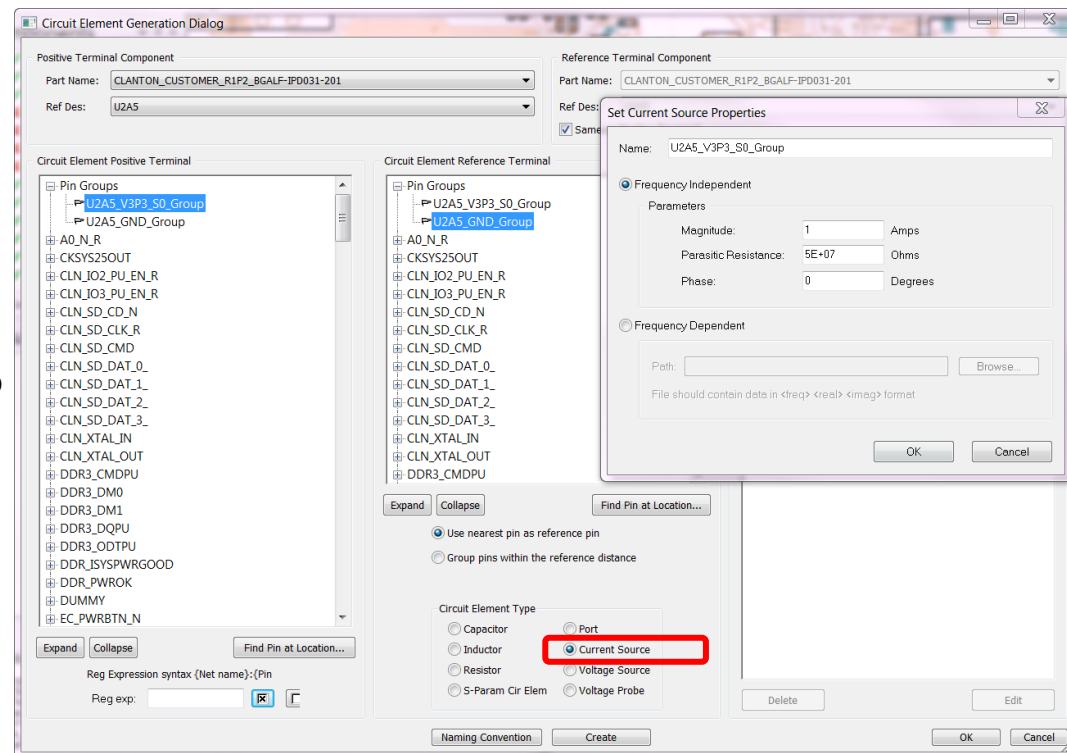
• Ports Creation

- In SIwave UI click and highlight the outline of BGA **U2A5** component
- Click the **Tools** tab and select **Generate Circuit Element on Components...**



- Circuit Element Positive Terminal
 - Pin Groups: **U2A5_V3P3_S0_Group**
- Circuit Element Reference Terminal
 - Pin Groups: **U2A5_GND_Group**
- Circuit Element Type:
 - **Current Source**
- Click: **Create**
- Set Current Source Properties:
 - Change Name to : **U2A5_V3P3_S0_Group**
 - **Magnitude: 1 Amps**
 - **Parasitic Resistance: 5e+07**
 - **Phase: 0 Degrees**
 - Click: **OK**
- Click: **OK**

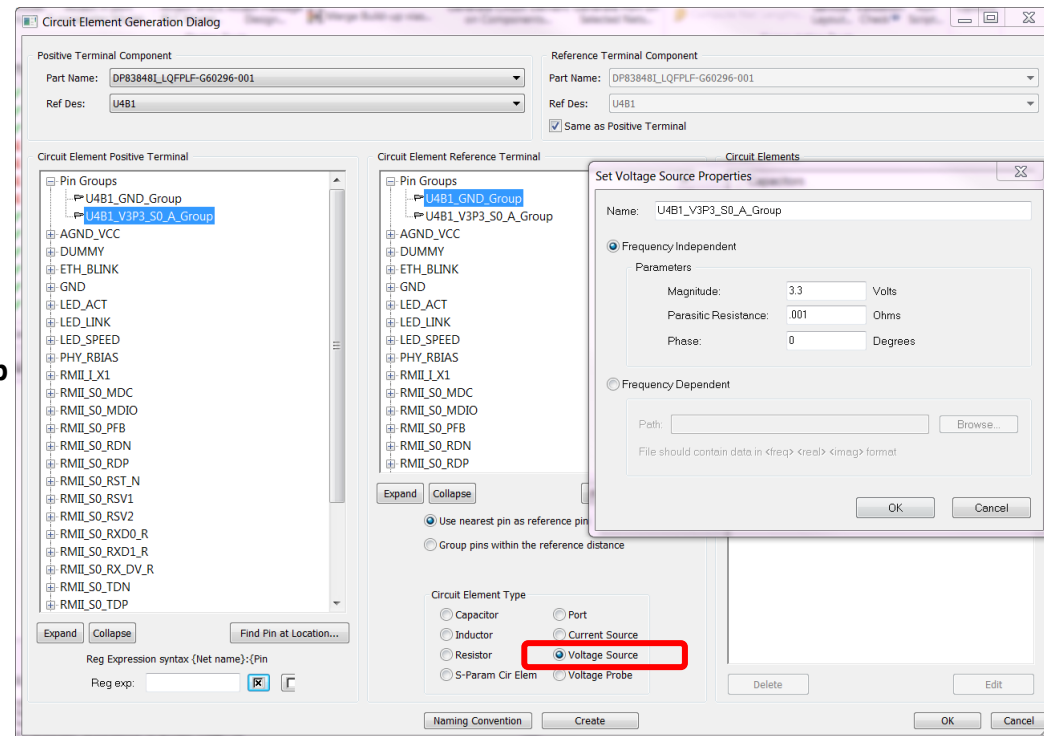
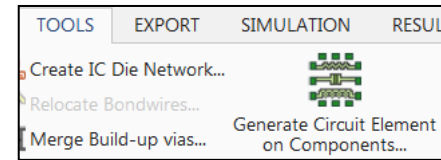
***Note – The Parasitic resistance is in parallel with the independent current source. This is a Norton Equivalent circuit**



Excitations (Ports)

• Ports Creation

- In SIwave UI click and highlight the outline of BGA **U4B1** component
- Click the **Tools** tab and select **Generate Circuit Element on Components...**
 - Circuit Element Positive Terminal
 - Pin Groups: **U4B1_V3P3_S0_A_Group**
 - Circuit Element Reference Terminal
 - Pin Groups: **U4B1_GND_Group**
 - Circuit Element Type:
 - **Voltage Source**
 - Click: **Create**
 - Voltage Source Properties:
 - Change Name to: **U4B1_V3P3_S0_A_Group**
 - **Magnitude: 3.3 Volts**
 - **Parasitic Resistance: 0.001**
 - **Phase: 0 Degrees**
 - Click: **OK**
 - Click: **OK**

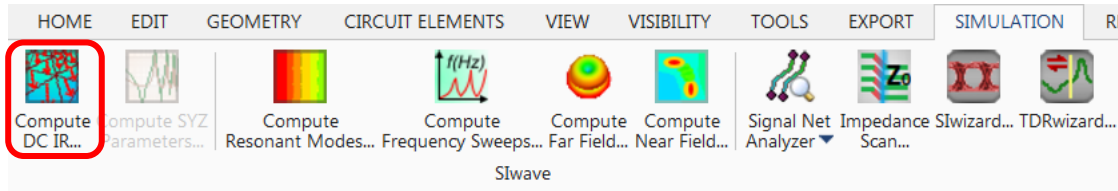


***Note – The Parasitic resistance is in series with the independent voltage source. This is a Thevenin Equivalent circuit. This resistance value will be included in the loop resistance, thus the reason to make it small**

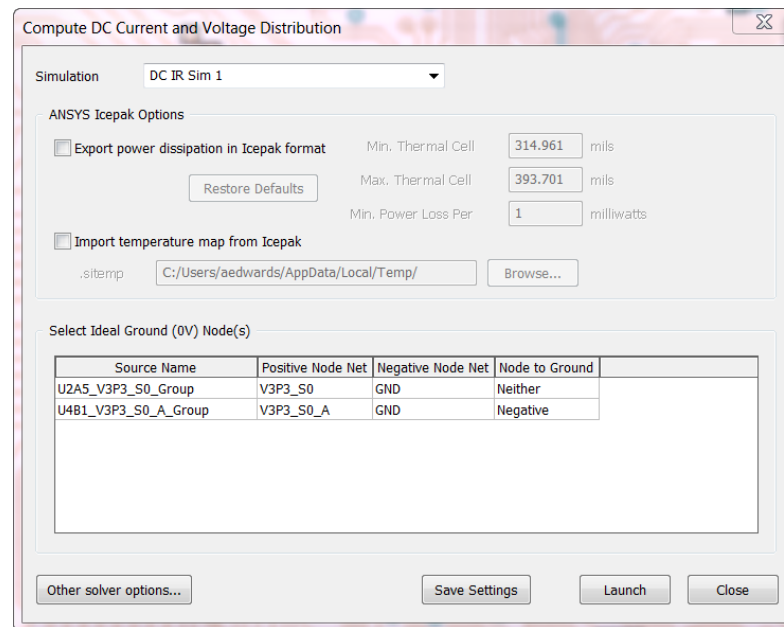
Setup the DC Current and Voltage Simulation

- **Configure the DC IR Drop Simulation**

- Click *Simulation > Compute DC IR*



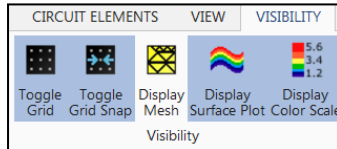
- Click the **Launch** button



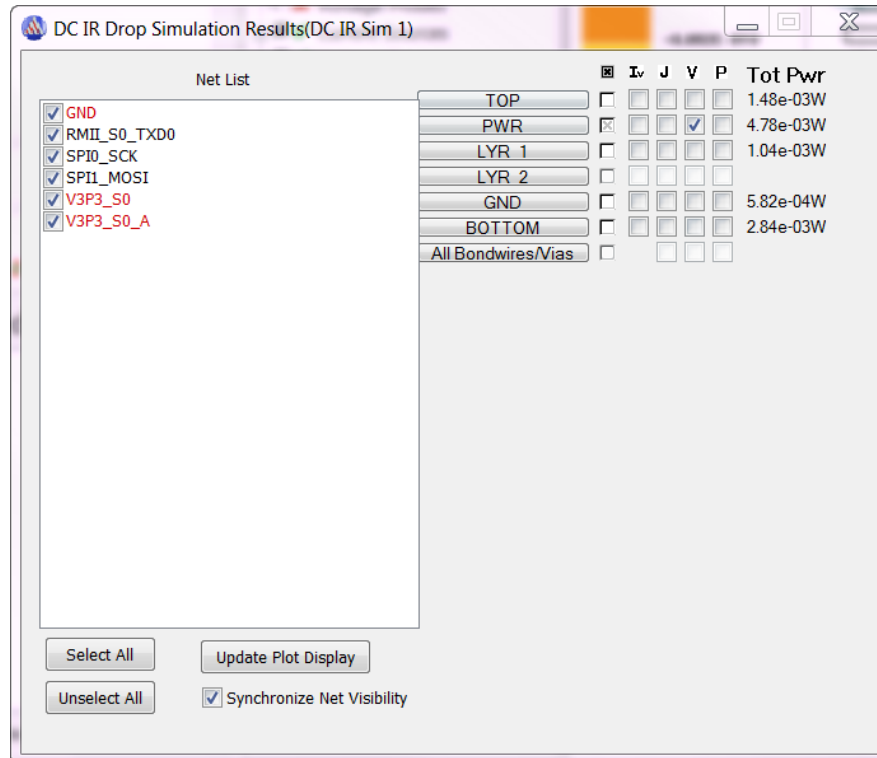
View DC Current and Voltage Results

- To view the DC Voltage Drop

- Turn off the Mesh display
 - Click **Visibility > Display Mesh**

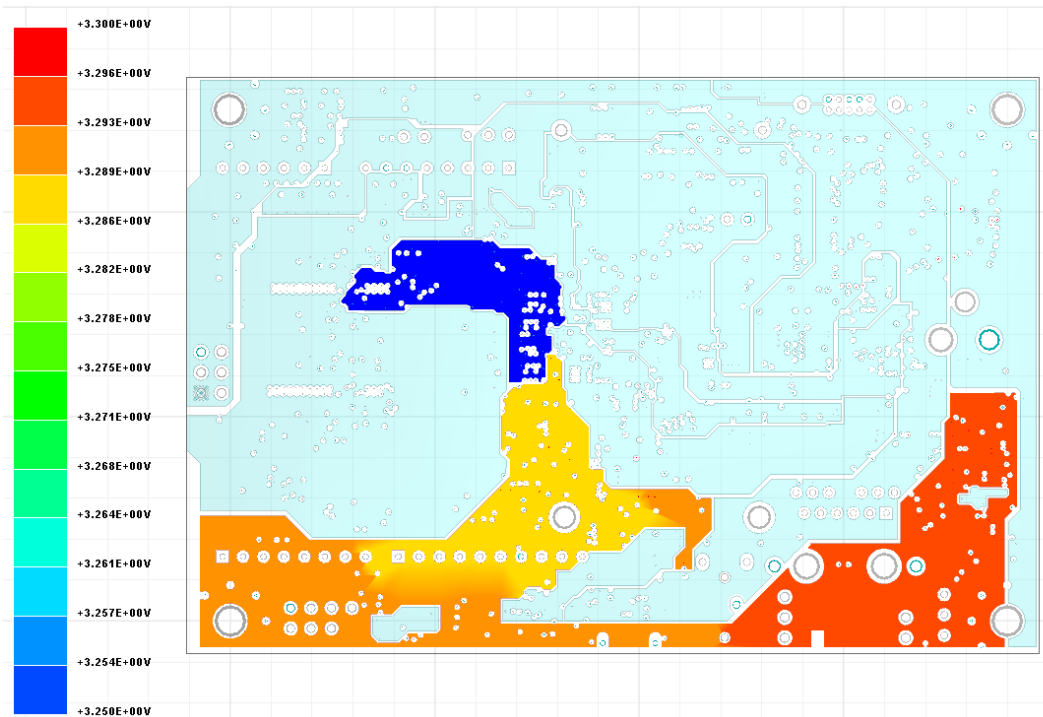
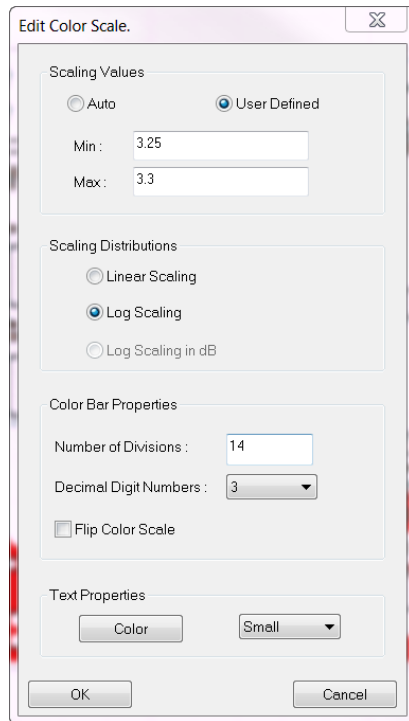


- Select **Results > DC IR Drop > DC IR Sim 1 > Currents/Voltages**
- Place a check mark for only:
 - Layer: **PWR**
 - Plot Type: **V**



View DC Current and Voltage Results

- To view the DC Voltage Drop
 - To change the color scale to show less voltage range
 - Double Click on the Color Scale
 - Scaling Values: **User Defined**
 - Min: **3.25**
 - Max: **3.3**
 - Click **OK**

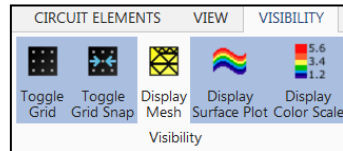


- Move the cursor around the power rail to view the voltage differences. Voltage should decrease the farther away from the VRM located at U4B1

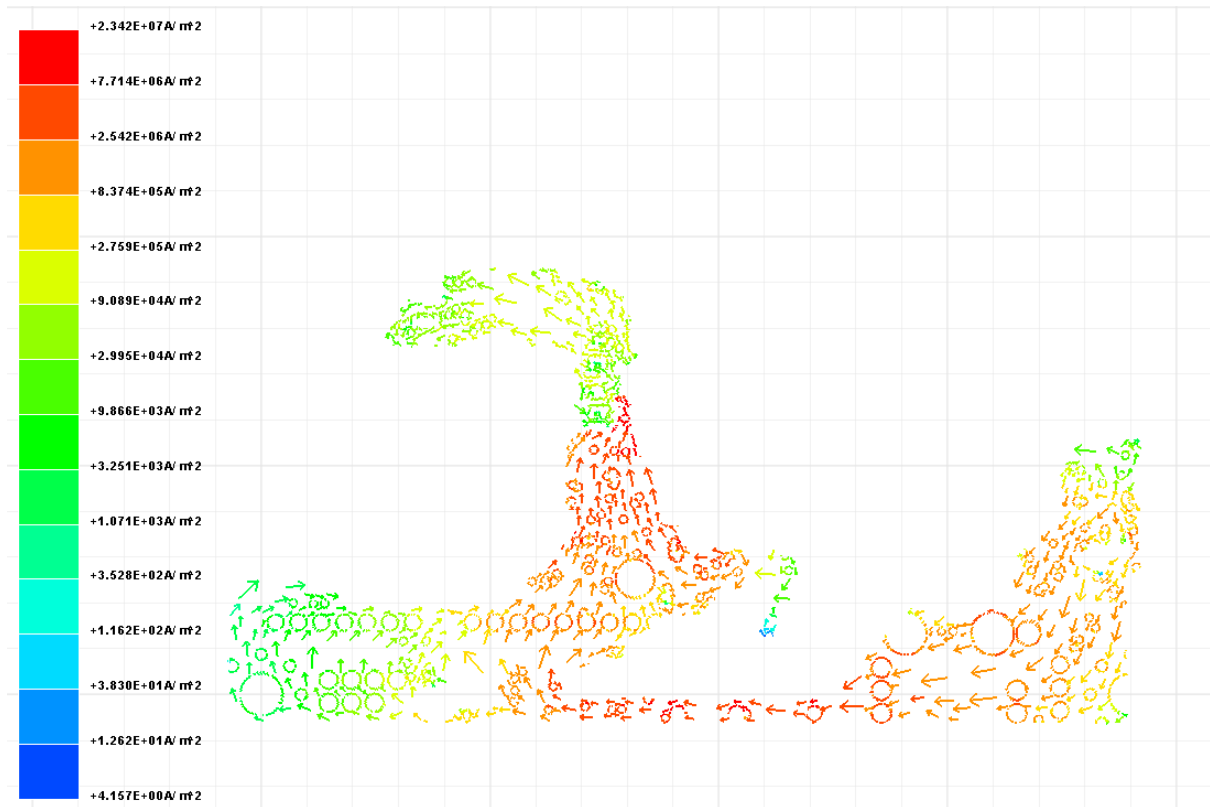
View DC Current and Voltage Results

- To view the Current Density and direction of flow

- Turn off the Mesh display
 - Click **Visibility > Display Mesh**



- Select **Results > DC IR Drop > DC IR Sim 1 > Currents/Voltages**
- Place a check mark for only:
 - Layer: **PWR**
 - Plot Type: **J**
- Close the Window



View DC Current and Voltage Results

- To view the Element Data
- Select **Results > DC IR DROP > DC IR SIM 1 > Element Data**
- Click the **Vias** tab
 - It shows pass or fail at each of the vias based upon default current limits or user supplied current limits.
 - Pass/Fail criteria is used to determine whether reliability issues will arise due to electromigration
- Click the **Voltage Source** tab
 - This shows the parallel current draw at the voltage source
- Click the **Current Source** tab
 - This shows the voltage at the current sink
- Click **Close**

DC Simulation Element Data(DC IR Sim 1)

Bondwires Current Sources Metallization **Vias** Voltage Probes Voltage Sources

Via	Net	x (mils)	y (mils)	Current / A	Limit / A	Pass / Fail	Resistance / Ohms
Via 0 (TOP-G...	GND	3.2500e+03	1.2080e+03	0.000000000000e+00	1.641732232276e+00	Pass	1.813762323980e-03
Via 0 (GND-B...	GND	3.2500e+03	1.2080e+03	0.000000000000e+00	1.641732232276e+00	Pass	1.404435419627e-04
Via 1 (TOP-G...	GND	3.3900e+03	1.7570e+03	-1.041137988789e-03	1.641732232276e+00	Pass	1.813762323980e-03
Via 1 (GND-B...	GND	3.3900e+03	1.7570e+03	0.000000000000e+00	1.641732232276e+00	Pass	1.404435419627e-04
Via 2 (TOP-G...	GND	2.2420e+03	1.0100e+03	0.000000000000e+00	1.641732232276e+00	Pass	1.813762323980e-03
Via 2 (GND-B...	GND	2.2420e+03	1.0100e+03	0.000000000000e+00	1.641732232276e+00	Pass	1.404435419627e-04
Via 3 (TOP-G...	GND	1.7580e+03	4.2700e+02	0.000000000000e+00	1.641732232276e+00	Pass	1.813762323980e-03
Via 3 (GND-B...	GND	1.7580e+03	4.2700e+02	0.000000000000e+00	1.641732232276e+00	Pass	1.404435419627e-04
Via 4 (TOP-G...	GND	3.0770e+03	2.5500e+03	0.000000000000e+00	1.380696807344e+01	Pass	2.156673393555e-04
Via 4 (GND-B...	GND	3.0770e+03	2.5500e+03	0.000000000000e+00	1.380696807344e+01	Pass	1.669958881840e-05
Via 5 (TOP-G...	GND	3.0270e+03	2.5500e+03	0.000000000000e+00	1.380696807344e+01	Pass	2.156673393555e-04
Via 5 (GND-B...	GND	3.0270e+03	2.5500e+03	0.000000000000e+00	1.380696807344e+01	Pass	1.669958881840e-05
Via 6 (TOP-G...	GND	3.3920e+03	2.5260e+03	0.000000000000e+00	1.641732232276e+00	Pass	1.813762323980e-03
Via 6 (GND-B...	GND	3.3920e+03	2.5260e+03	0.000000000000e+00	1.641732232276e+00	Pass	1.404435419627e-04
Via 7 (TOP-G...	GND	2.9270e+03	2.5500e+03	0.000000000000e+00	1.380696807344e+01	Pass	2.156673393555e-04
Via 7 (GND-B...	GND	2.9270e+03	2.5500e+03	0.000000000000e+00	1.380696807344e+01	Pass	1.669958881840e-05
Via 8 (TOP-G...	GND	2.4340e+03	2.6090e+03	0.000000000000e+00	1.641732232276e+00	Pass	1.813762323980e-03
Via 8 (GND-B...	GND	2.4340e+03	2.6090e+03	0.000000000000e+00	1.641732232276e+00	Pass	1.404435419627e-04
Via 9 (TOP-G...	GND	2.1820e+03	2.6090e+03	0.000000000000e+00	1.641732232276e+00	Pass	1.813762323980e-03
Via 9 (GND-B...	GND	2.1820e+03	2.6090e+03	0.000000000000e+00	1.641732232276e+00	Pass	1.404435419627e-04
Via 10 (TOP-...	GND	2.2120e+03	2.6090e+03	0.000000000000e+00	1.641732232276e+00	Pass	1.813762323980e-03

Fit Selection

Export Close

DC Simulation Element Data(DC IR Sim 1)

Bondwires Current Sources Metallization **Vias** Voltage Probes Voltage Sources

Source Name	Current / A	Series R Voltage / V
U4B1_V3P3_S0_A_Gro...	1.000358738161e+00	1.000358738161e-03

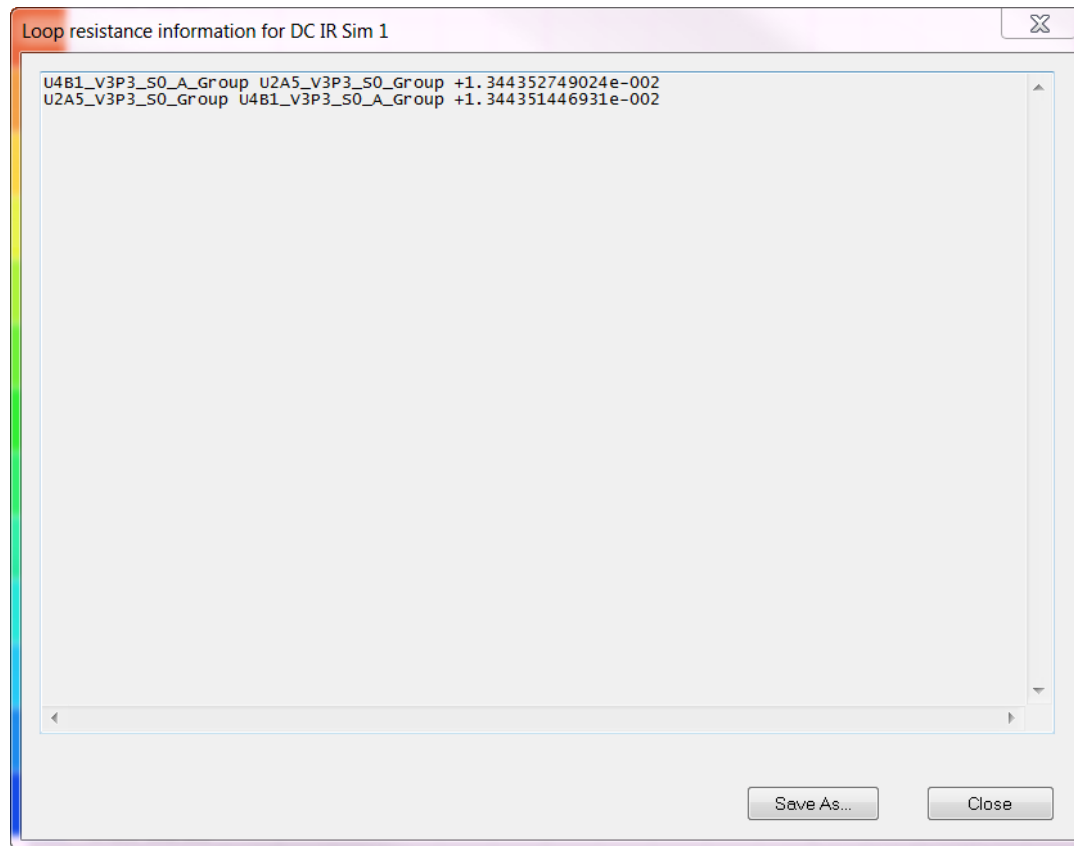
DC Simulation Element Data(DC IR Sim 1)

Bondwires **Current Sources** Metallization Vias Voltage Probes Voltage Sources

Source Name	Parallel R Current / A	Voltage / V
U2A5_V3P3_S0_Group	6.571104218326e-08	3.285552109163e+00

View DC Current and Voltage Results

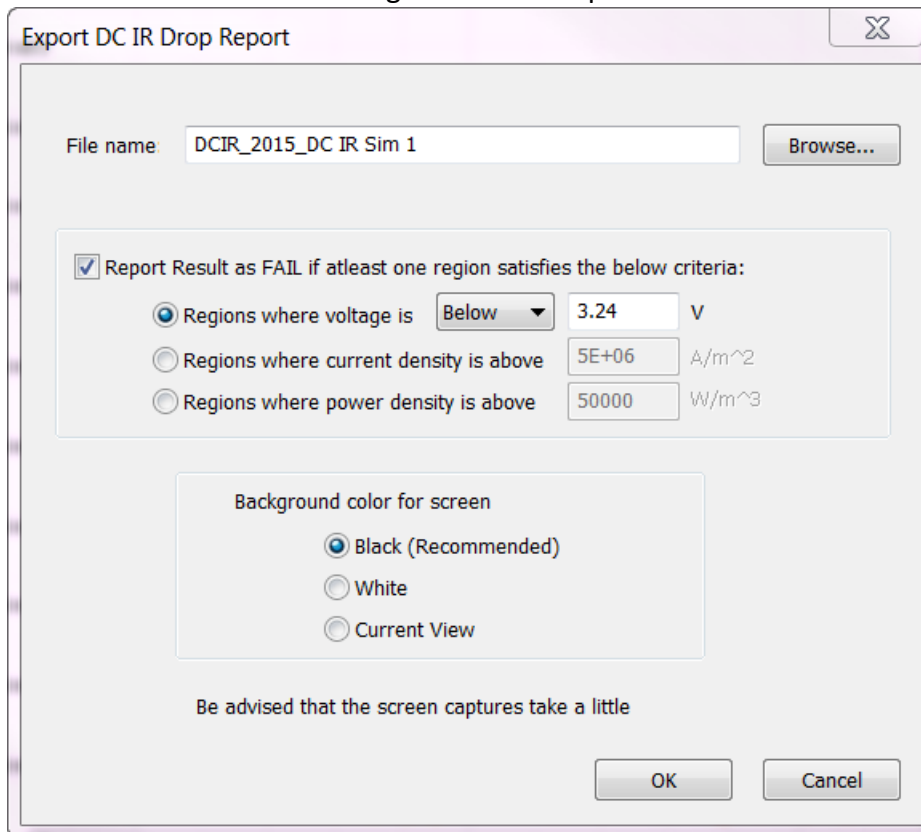
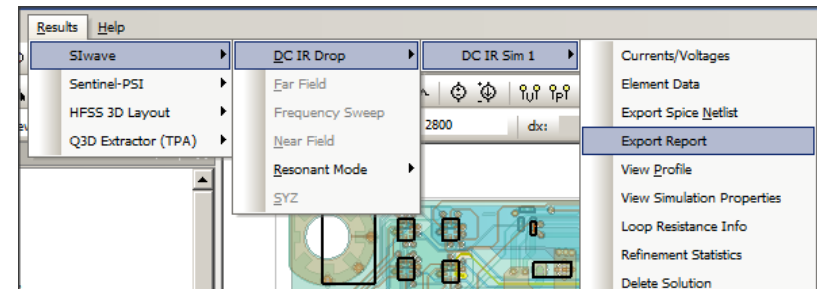
- To view the Loop Resistance
- Select **Results > DC IR DROP > DC IR SIM 1 > Loop Resistance Info**
- Click **Close**



Generate a DC IR Drop Report

• Creating a Voltage/Current Report

- After a DC IR drop simulation has been run, a HTML report can be created detailing the simulation results.
- Select **Results > DC IR DROP > DC IR SIM 1 > Export Report**
 - Place check mark next to **Report Results as Fail if at least...**
 - Regions where voltage is: **Below 3.24V**
- Click on the **OK** button to generate the report.



DC IR Drop Simulation Report

Siwave Version: 2015.0.0
 Creation Date: Tue Jan 13 11:57:12 2015
 Design File: DCIR_2015.siw
 Simulation Name: DC IR Sim 1

Layer Stack-up

Name	Type	Thickness(mils)	Material	Conductivity(S/m)	Dielectric Constant	Loss Tangent	Transducency	Elevation(mils)	Roughness(mils)	Current Plot	Voltage Plot
UNNAMED_1	DIELECTRIC		CDS_AIR	0	1	0		80.1			
TOP	METAL	1.9	CDS_COOPER0.959E+07	1	0	0	65	78.2	HJ: 0, HJ: 0	→	→
UNNAMED_3	DIELECTRIC	2.65	CDS_FR-4	0	3.86	0.024		75.55			
PWR	METAL	1.3	CDS_COOPER0.959E+07	1	0	0	65	74.25	HJ: 0, HJ: 0	→	→
UNNAMED_5	DIELECTRIC	50	CDS_FR-4.1	0	4.34	0.018		24.25			
LYR_1	METAL	1.2	CDS_COOPER0.959E+07	1	0	0	65	23.05	HJ: 0, HJ: 0	→	→
UNNAMED_7	DIELECTRIC		CDS_FR-4.2	0	4.5	0.035		15.05			
LYR_2	METAL	1.2	CDS_COOPER0.959E+07	1	0	0	65	13.85	HJ: 0, HJ: 0		
UNNAMED_9	DIELECTRIC		CDS_FR-4.2	0	4.5	0.035		5.85			
GND	METAL	1.3	CDS_COOPER0.959E+07	1	0	0	65	4.55	HJ: 0, HJ: 0	→	→
UNNAMED_11	DIELECTRIC	2.65	CDS_FR-4	0	3.86	0.024		1.9			
BOTTOM	METAL	1.9	CDS_COOPER0.959E+07	1	0	0	65	0	HJ: 0, HJ: 0	→	→
UNNAMED_13	DIELECTRIC		CDS_AIR	0	1	0		0			

Generate a DC IR Drop Report

• View the Report

- After the report generation has completed navigate to the project folder and open:

- **DCIR_DC IR Sim 1.htm**
- The file can be opened in any web browser or HTML viewer.

- When finished exploring the report close the document.

Note: This report can be customized based on user defined criteria and can be used to highlight areas of concern in the design.

- Save the Siwave project:

- **File > Save**

DC IR Drop Simulation Report

Siwave Version: 2015.0.0

Creation Date: Tue Jan 13 11:57:12 2015

Design File: DCIR_2015.siw

Simulation Name: DC IR Sim 1

Layer Stack-up

Name	Type	Thickness(mils)	Material	Conductivity(S/m)	Dielectric Constant	Loss Tangent	Translucency	Elevation(mils)	Roughness(mils)	Current Plot	Voltage Plot	Power Plot
UNNAMED_1	DIELECTRIC	0	CDS_AIR	0	1	0		80.1				
TOP	METAL	1.9	CDS_COPPER	5.959E+07	1	0	65	78.2	HJ: 0, HJ: 0	→	→	→
UNNAMED_3	DIELECTRIC	2.65	CDS_FR-4	0	3.86	0.024		75.55				
PWR	METAL	1.3	CDS_COPPER	5.959E+07	1	0	65	74.25	HJ: 0, HJ: 0	→	→	→
UNNAMED_5	DIELECTRIC	50	CDS_FR-4	1	4.34	0.018		24.25				
LYR_1	METAL	1.2	CDS_COPPER	5.959E+07	1	0	65	23.05	HJ: 0, HJ: 0	→	→	→
UNNAMED_7	DIELECTRIC	8	CDS_FR-4	2	4.5	0.035		15.05				
LYR_2	METAL	1.2	CDS_COPPER	5.959E+07	1	0	65	13.85	HJ: 0, HJ: 0			
UNNAMED_9	DIELECTRIC	8	CDS_FR-4	2	4.5	0.035		5.85				
GND	METAL	1.3	CDS_COPPER	5.959E+07	1	0	65	4.55	HJ: 0, HJ: 0	→	→	→
UNNAMED_11	DIELECTRIC	2.65	CDS_FR-4	0	3.86	0.024		1.9				
BOTTOM	METAL	1.9	CDS_COPPER	5.959E+07	1	0	65	0	HJ: 0, HJ: 0	→	→	→
UNNAMED_13	DIELECTRIC	0	CDS_AIR	0	1	0		0				

<input type="checkbox"/>	Current Plot	<input type="checkbox"/>	Voltage Plot	<input type="checkbox"/>	Power Plot
<input type="checkbox"/>	VIA	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Plots grouped by: Plot Type [\(Switch to group by Layer\)](#)

Current Sources

Simulation Results									
Name	Initial Setup					Simulation Results			
	Magnitude(A)	Phase(degrees)	Source Resistance(ohms)	Positive Terminal Net	Negative Terminal Net	Positive Terminal	Negative Terminal	Parallel R Current(A)	Voltage(V)
U2A5_V3P3_50_Group1	1	0	5E+07	V3P3_50	GND	U2A5_V3P3_50_Group(U2A5)	U2A5_GND_Group(U2A5)	6.571104218326e-08	3.285552109163e+00

Voltage Sources

Initial Setup								Simulation Results	
Name	Magnitude(V)	Phase(degrees)	Source Resistance(ohms)	Positive Terminal Net	Negative Terminal Net	Positive Terminal	Negative Terminal	Current(A)	Series R Voltage(V)
U4B1_V3P3_50_A_Group3.3	3.3	0	0.001	V3P3_50_A	GND	U4B1_V3P3_50_A_Group(U4B1)	U4B1_GND_Group(U4B1)	1.000358738161e+00	0.000358738161e-03

Results Info

Result: FAIL